NXD1005/1006

Voice Player with Digital Amplifier & Flash

General Description

The NXD1005/1006 is an 4bit-ADPCM codec Voice player.
It includes Digital amplifier and enable to drive 6～16 ohm speaker directly.
The NXD1005 is a non flash memory version and the NXD1006 is an embedded flash memory version.
All of them can extend external flash memory.
The NXD1005/1006 can be used Stand alone mode or u-Com mode.

Feature

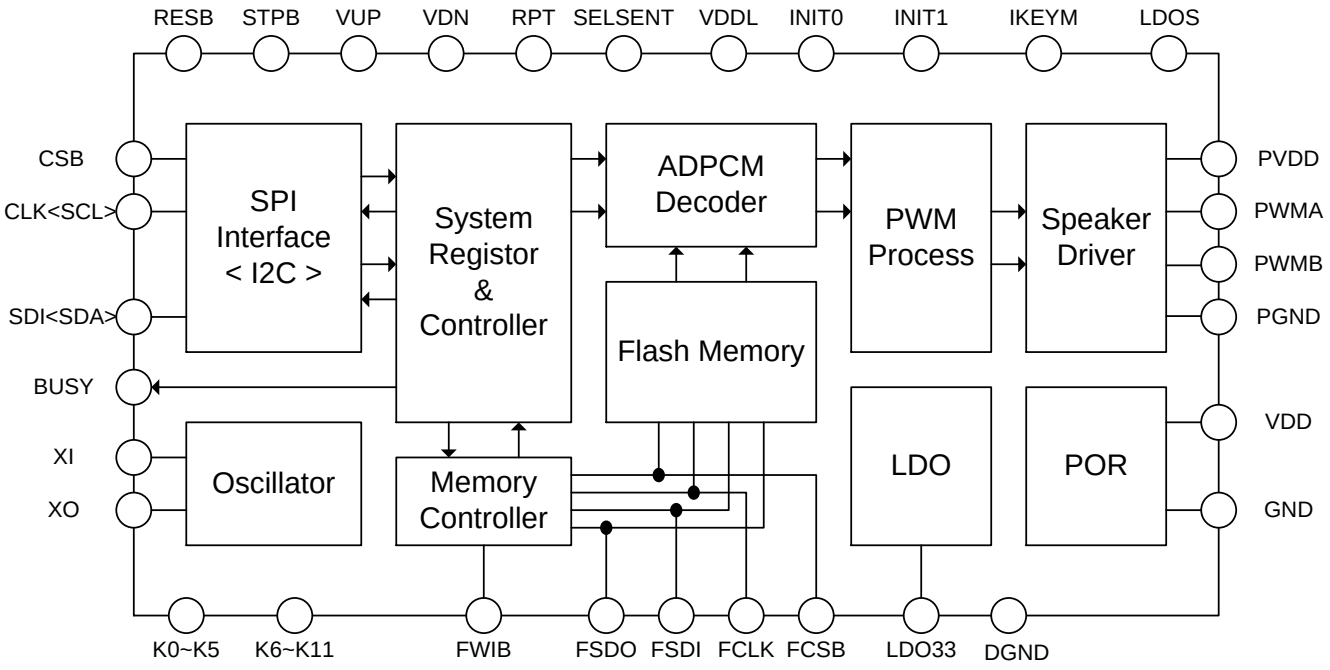
- Supply voltage : 2.8V ~ 5.5V
- 16bits operation in ADPCM Decoder
- Stand alone / SPI, I2C control interfaces
- Program play : Selectable Phrase play or Sentence play
- Direct play : PCM or 4bit-ADPCM input
- Non-Encoded data can be saved in the Internal/external flash memory for high quality.
- Direct internal/external serial flash memory access
- Direct speaker drive with internal Digital amplifier
  600mW @ 8ohm, THD=10% (VCC=3.3V)
  1.5W @ 8ohm, THD=10% (VCC=5.5V)
- X-tal oscillator or OSC : Master clock Frequency is 16.384MHz, 24.576MHz or 32.768MHz
- RC oscillator : 16.384MHz
- Maximum 36 keys(matrix structure) at stand alone mode
- Sampling rate : 4, 8, 16KHz / 6, 12, 24KHz / 8, 16, 32KHz
  (X-tal : 16.384MHz / 24.576MHz / 32.768MHz)
- Maximum play time (@ internal 8M, 4K Sampling rate, 4bit-ADPCM) : 500sec
- Built in a Low Dropout Regulator
- Built in Power on reset
- A few external parts
- Package : 24SOP, 44QFP(Not manufactured)

Application

- Toys
- GPS, Navigation
- Audio book
- Answering machine
- Home voice applications

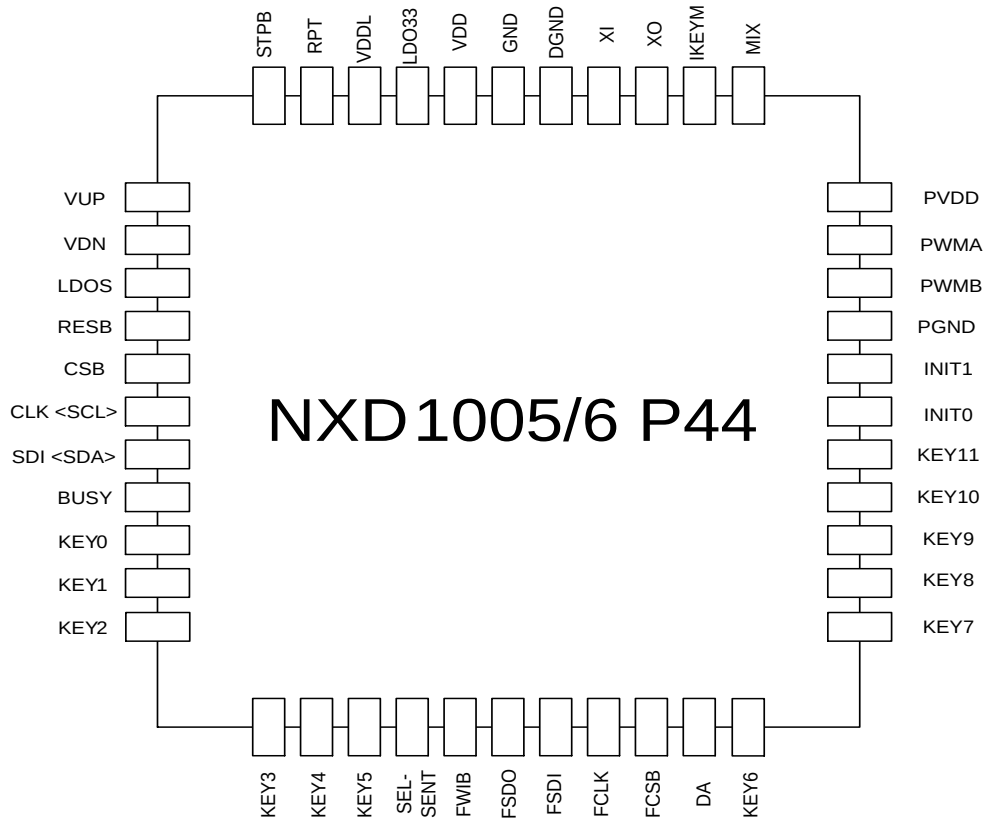
Block Diagram (44QFP)

※ <> : for I2C interface



Terminal Assignment – For Stand Alone mode and MCU mode (44QFP)

※ <> : for I2C interface



Pin description (44QFP)

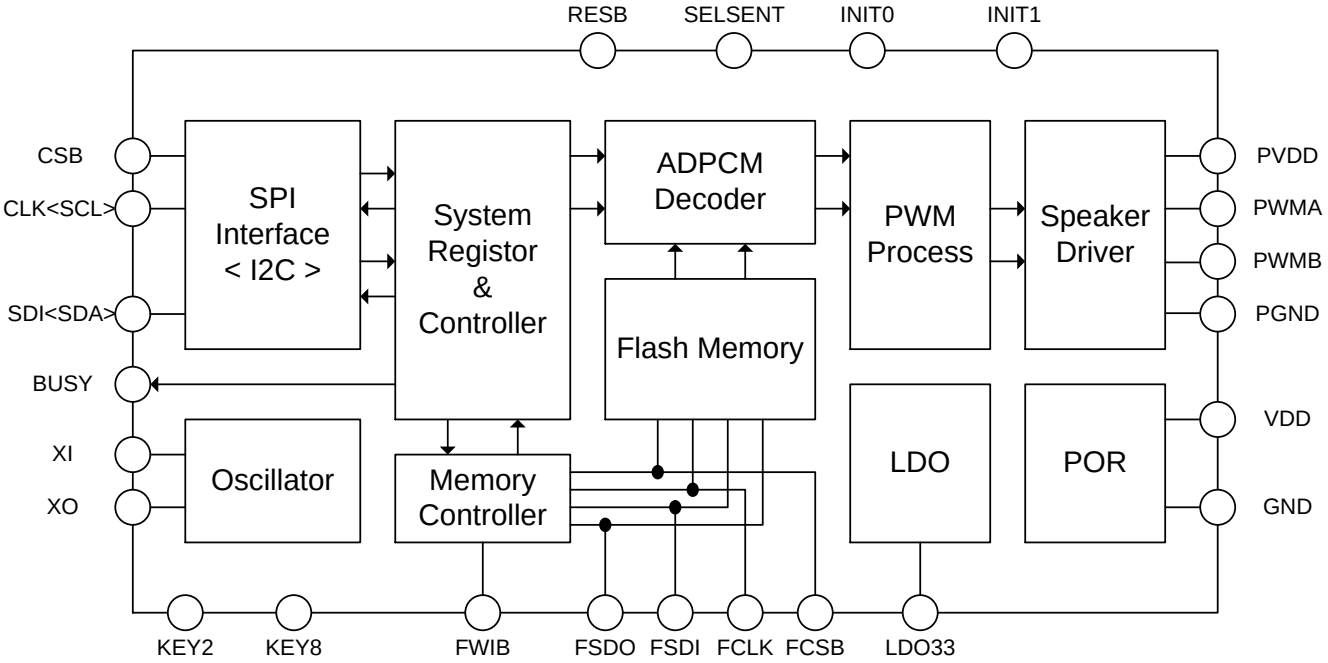
※ <> : for I2C interface

Pin Name	Pin No.	I/O	Description	PU/PD
VUP	1	I	Volume up pin (for Stand alone)	PU
VDN	2	I	Volume down pin (for Stand alone)	PU
LDOS	3	I/O	※ Must Connected to Vin	-
RESB	4	I	Reset pin	PU
CSB	5	I	SPI enable	PU
CLK <SCL>	6	I	SPI clock <Serial Clock Line>	-
SDI <SDA>	7	I	SPI Data input <Serial Data>	-
BUSY	8	O	Flash programmable BUSY signal. Active Low	-
KEY0	9	I	Input key0 for selecting phrase	PU
KEY1	10	I	Input key1 for selecting phrase	PU
KEY2	11	I	Input key2 for selecting phrase	PU
KEY3	12	I	Input key3 for selecting phrase	PU
KEY4	13	I	Input key4 for selecting phrase	PU
KEY5	14	I	Input key5 for selecting phrase	PU
SELSENT	15	I	Play mode selection pin(0:phrase,1:sentence)	-
FWIB	16	O	External flash memory write inhibit output	-
FSDO	17	O	Serial data input of the external flash memory	-
FSDI	18	I	Serial data output of the external flash memory	PD
FCLK	19	O	External flash memory clock	-
FCSB	20	O	External flash memory chip select signal	-
DA	21	I	DA mode (0 :normal operation 1:DA Mode)	-
KEY6	22	I/O	Input key6 for selecting phrase (IKEYM:1) /Output key1 for selecting phrase (IKEYM:0)	-
KEY7	23	I/O	Input key7 for selecting phrase (IKEYM:1) /Output key2 for selecting phrase (IKEYM:0)	-
KEY8	24	I/O	Input key8 for selecting phrase (IKEYM:1) /Output key3 for selecting phrase (IKEYM:0)	-
KEY9	25	I/O	Input key9 for selecting phrase (IKEYM:1) /Output key4 for selecting phrase (IKEYM:0)	-
KEY10	26	I/O	Input key10 for selecting phrase (IKEYM:1) /Output key5 for selecting phrase (IKEYM:0)	-
KEY11	27	I/O	Input key11 for selecting phrase (IKEYM:1) /Output key6 for selecting phrase (IKEYM:0) /Playing Status Monitor Pin	-
INIT0	28	I/O	Initial volume setting pin 0 Output when Playing Status Monitor Option	-
INIT1	29	I/O	Initial volume setting pin 1 Output when Playing Status Monitor Option	-
PGND	30	G	Power ground	-
PWMB	31	O	PWM out B	-

PWMA	32	O	PWM out A	-
PVDD	33	P	Power VDD	-
MIX	34	I	MIX Mode	-
IKEYM	35	I	I/O Key mode select pin(0:matrix,1:direct)	PD
XO	36	O	X-tal oscillator output	-
XI	37	I	X-tal oscillator input	-
DGND	38	G	Digital ground	-
GND	39	G	Analog ground	-
VDD	40	P	Analog VDD (for LDO)	-
LDO33	41	O	LDO 3.3V output	-
VDDL	42	I	Digital power (Connect to LDO33(Pin #41) Or Power 3.3V)	-
RPT	43	I	Repeat circulation in phrase mode	PU
STPB	44	I	Play stop control pin	PU

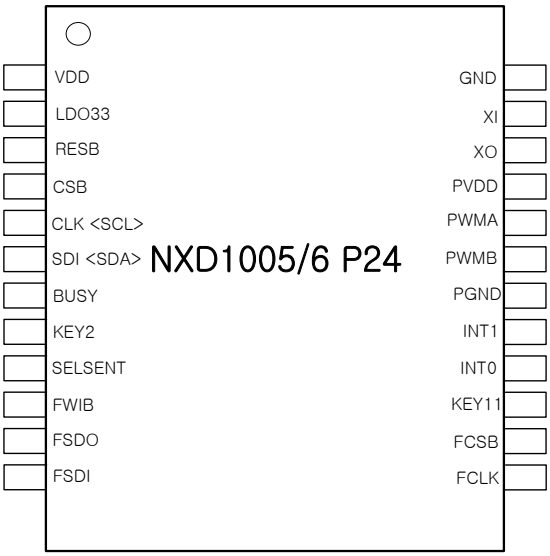
Block Diagram (24SOP)

※ <> : for I2C interface



Terminal Assignment (24SOP)

※ <> : for I2C interface



Pin Name	Pin No.	I/O	Description	PU/PD
VDD	1	P	Analog VDD (for LDO)	-
LDO33	2	O	LDO 3.3V output	-
RESB	3	I	Reset pin	PU
CSB	4	I	SPI enable	PU
CLK <SCL>	5	I	SPI clock <Serial Clock Line>	-
SDI <SDA>	6	I	SPI Data input <Serial Data>	-
BUSY	7	O	Flash programmable BUSY signal. Active Low	-
KEY2	8	I	For Operating Status Monitor	PU
SELSENT	9	I	Play mode selection pin(0:phrase,1:sentence)	-
FWIB	10	O	External flash memory write inhibit output	-
FSDO	11	O	Serial data input of the external flash memory	-
FSDI	12	I	Serial data output of the external flash memory	PD
FCLK	13	O	External flash memory clock	-
FCSB	14	O	External flash memory chip select signal	-
KEY11	15	O	Output key6 for selecting phrase /Playing Status Monitor Pin	-
INIT0	16	I/O	Initial volume setting pin 0 Output when Playing Status Monitor Option	-
INIT1	17	I/O	For Playing Status Monitor	-
PGND	18	G	Power ground	-
PWMB	19	O	PWM out B	-
PWMA	20	O	PWM out A	-
PVDD	21	P	Power VDD	-
XO	22	O	X-tal oscillator output	-
XI	23	I	X-tal oscillator input	-
GND	24	G	Ground	-

Maximum Absolute ratings

Parameter	Symbol	Value	Unit
Supply Voltage	Vccmax	-0.3 ~ 6.0	V
Storage temperature	Tstg	-45 ~ 150	℃
Operating temperature	Topr	-40 ~ 85	℃
Power Dissipation	Pdmax	800	mW

ESD Characteristics

Mode	Polarity	Characteristic			Unit
		min	typ	max	
HBM	Positive/Negative	2000	-	-	V
MM	Positive/Negative	200	-	-	V
CDM	Positive/Negative	800	-	-	V

Electrical Characteristics

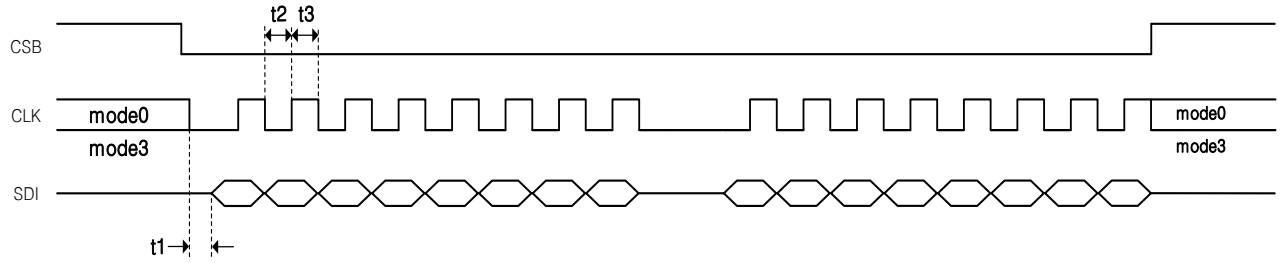
VCC = 5.0V, Ta=25.0℃ Unless otherwise noted

Characteristics	Symbo	Condition	Value			Unit
			min	typ	max	
Operating voltage range	Vop	-	2.8	-	5.5	V
Stand by current	Ist	Vin=5.0V	-	1.4	2.0	mA
Output Power	Po	8ohm, 10%, VIN=3.3V	500	600	-	mW
LDO output voltage	Vout	Vin=5.0V	3.0	3.3	3.6	V
Total harmonic distortion + N	THD+N	8ohm, Po=40mW, 1KHz	-	10	-	%
Volume control range	Rvol	-	-98	-	+0	dB
Initial Setting Time(*)	TINIT	-		200		ms

* After NXD1005/6 is reset or power on, you should wait for Initial Setting Time.
Initial Setting Time is for reading internal flash information and setting initial volume.

Timing Diagram

- SPI Timing (CSB, CLK, SDI)

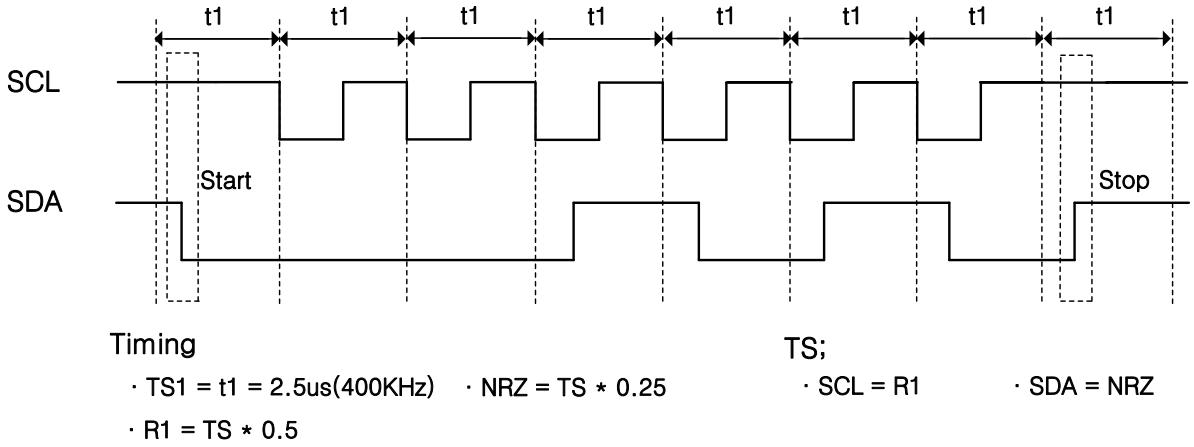


It`s not necessary to consider status of the CLK(mode0 or mode3) when CSB is high in this interface.

Parameter	Symbol	min	typ	max	Unit
SDI Setup Time	t1	5	-	20	ns
CLK Clock Low Period	t2	500	-	-	ns

CLK Clock High Period	t3	500	-	-	ns

- I2C Timing (SCL, SDA)



Timing

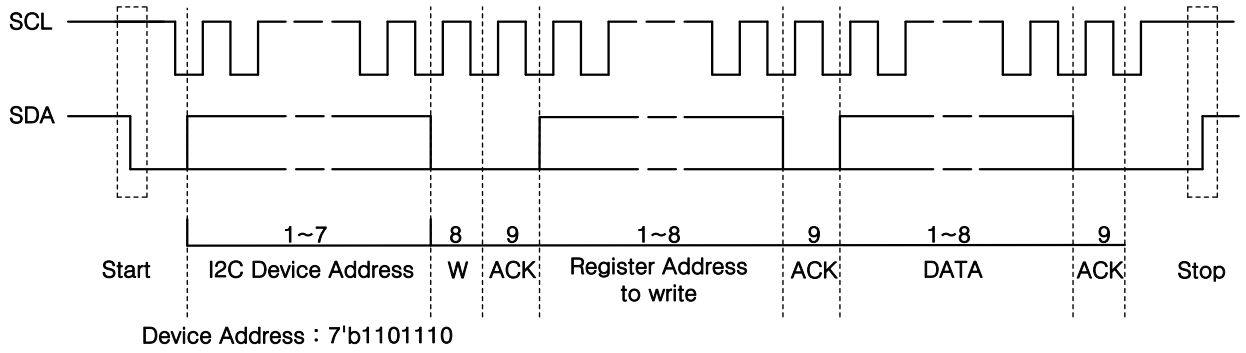
· TS1 = t1 = 2.5us(400KHz) · NRZ = TS * 0.25

· R1 = TS * 0.5

TS;

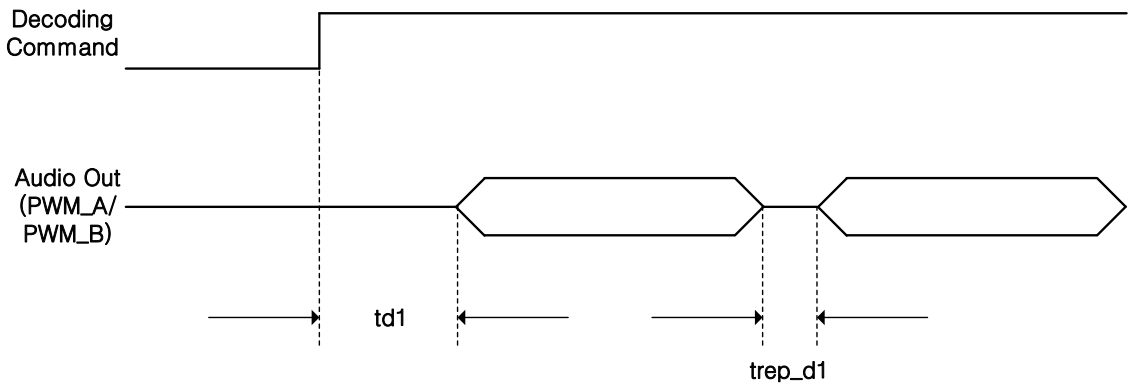
· SCL = R1 · SDA = NRZ

- The timing flow of write mode is same below figure



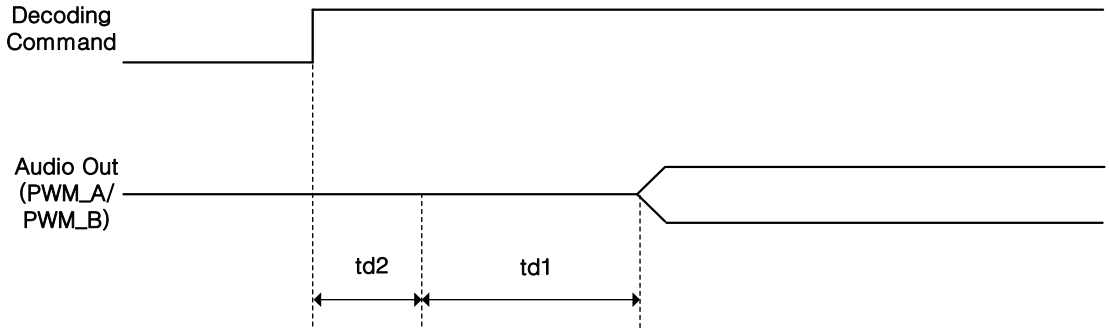
Device Address : 7'b1101110

- Decode timing (Using internal flash memory mode)



The td1 is the time-gap between the stat command for decode and the real audio output.

- Decode timing (Using external flash memory mode)



Parameter	Symbol	fs=4KHz	fs=8KHz	fs=16KHz	comments
Data out delay	td1	32ms	16ms	8ms	-
FIFO buffer delay	td2	-	-	-	*1
Blank period in repeat mode	trep_d1	16ms	8ms	4ms	repeat mode

*1 : The td2 is the data downloading time from the External Memory to FIFO buffer.
NXD1005/6 has the 256 byte FIFO for the data buffer.

Sampling Rate

NXD1005/1006 can play non-encoded or encoded data (ADPCM). NXD1005/1006 supplies normally 4, 8, 16KHz sampling rate by using 16.384MHz in system clock. Also NXD1005/1006 supports 6, 12, 24KHz and 8, 16, 32KHz in the option. You should use 24.576MHz in system clock for 6, 12, 24KHz sampling rate and 32.768MHz for 8, 16, 32KHz sampling rate. In case that you use 32KHz sampling rate, we recommend non-encoded data for much better sound quality. Because non-encoded is fewer noise than encoded data (ADPCM).

Register Map

Name	Addr	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
Phrase Number1	$E0h	0~254 Phrase / 0~255 Sentence								0x00
Volume	$E1h	Volume (+0~-96dB)								※Setting by INIT0 and INIT1 Pin Status.
Control0	$E2h	-			Stop	Repeat[1:0]		OprMode[1:0]		0x00
Control1	$E3h	EnDth	SymDth	AmtDth[1:0]		EnFlt	-			0x00
Phrase Number2	$E4h	-		Phrase Group[2:0]			256 ~ 2047 Sentence			0x00

※ Refer to Initial Volume Chart to P.11.

- Phrase Number Register ($E0h & $E4h)

This register designates the phrase number or sentence number for decoding.
There are 8 groups of 255 phrases. You can select phrase group by setting E4h register.
There are 2048 sentences that are combined with 8 phrases.
You can play voice and music by setting E0h register

- Volume Control Register ($E1h)

This register controls the volume of the signal.

Number	Volume[dB]	Number	Volume[dB]	Number	Volume[dB]	Number	Volume[dB]
18h	0	19h	-1	1ah	-2	1bh	-3
1ch	-4	1dh	-5	1eh	-6	1fh	-7
20h	-8	21h	-9	22h	-10	23h	-11
24h	-12	25h	-13	26h	-14	27h	-15
28h	-16	29h	-17	2ah	-18	2bh	-19
2ch	-20	2dh	-21	2eh	-22	2fh	-23
30h	-24	31h	-25	32h	-26	33h	-27
34h	-28	35h	-29	36h	-30	37h	-31
38h	-32	39h	-33	3ah	-34	3bh	-35
3ch	-36	3dh	-37	3eh	-38	3fh	-39
40h	-40	41h	-41	42h	-42	43h	-43
44h	-44	45h	-45	46h	-46	47h	-47
48h	-48	49h	-49	4ah	-50	4bh	-52
4ch	-54	4dh	-56	4eh	-58	4fh	-60
50h	-64	51h	-68	52h	-72	53h	-78
54h	-84	55h	-90	56h	-96	57h	-98

※ Volume Data 00h ~ 17h Do not use

- Control0 Register ($E2h)

OprMode (Operating Mode) :
You can select operating Mode by setting these two bits.

0h : Nomal Play from Internal/External flash memory.
1h : Internal/External Flash Memory Program Mode.
2h : Direct Play Mode (etc. : PC control program)

Repeat :

This two bits register is for the repetition play for the selected phrase or sentence.

0h : 1-time play　　1h : 2-time play

2h : 4-time play　　3h : endless play until stop

Stop :

If you want to stop during playing, you can stop play by setting this register high. It is not necessary to reset because it is internally cleared oneself.

- Control1 Register (D-Amp Control Register)

EnDth :

It will use a dither function for sound quality improvement.

0: Disable, 1: Enable

SynDth :

Select dither function mode.

0: Asymmetrical, 1: Symmetrical

AmtDth :

Set the amount of dither.

0h: 18-bit position, 1h: 17-bit position, 2h: 16-bit position, 3h 15-bit position.

EnFlt :

Set the activation of fault protection function in the Speaker Block.

0: Disable, 1: Enable

Common Operation

- Internal / External OSC

NXD1005/6 combines RC OSC (16MHz). To use the internal RC OSC, user has to make the XI pin(44QFP-#37, 24SOP-#23) connected to VCC. For using X-tal, connect it to XI pin input and RC OSC will be stopped.

- Initial Volume Control

The initial volume level is controlled by the INIT0, INIT1 pin at power on time.

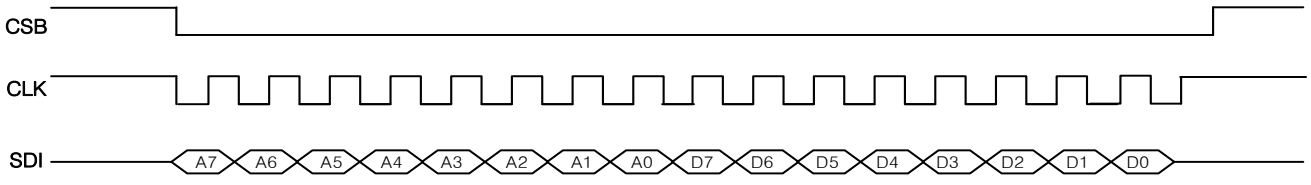
INIT1	INIT0	Volume(dB)	Number
0	0	0	18h
0	1	-6	1eh
1	0	-12	24h
1	1	-18	2ah

Initial Volume Chart

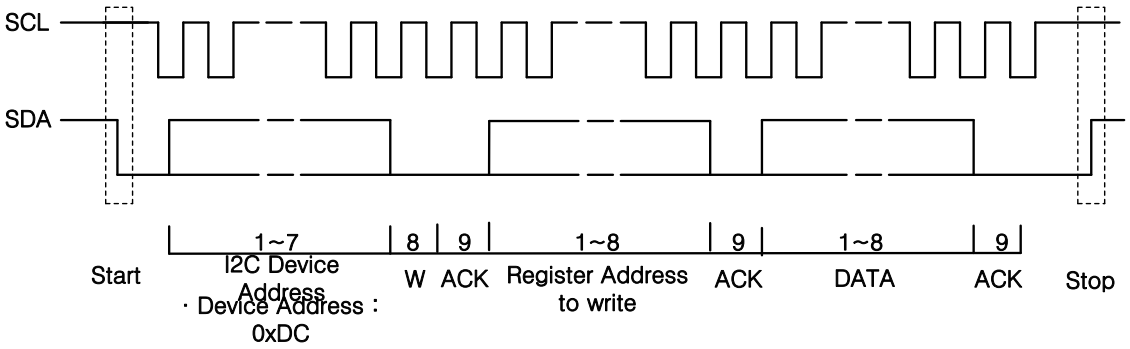
- DA (Digital to Analog) Option

In state of Pin is “Low”, it operates normal (Not DA option),
To use DA option, make Pin DA(44QFP-#21) High-Level. Line-out of PWMA will be output.

- MCU Operation by SPI and I2C I/F



SPI I/F Timing Chart



I2C I/F Timing Chart

The above is the timing diagram of SPI and I2C interfaces. The structure of SPI is composed with the 8 bits address and the 8 bits data. With these interfaces, MCU controls all the operations. The register control by using the MCU I/F is referenced the Register Map. MCU interface protocol is automatically detected without any pin configurations.

In the SPI interface, CSB(44QFP-#5, 24SOP-#4) goes to High level status for next command. And this CSB signal must be High status during minimum 3us for the stable operation of NXD1005/6. For the decoding operation, MCU must observe the BUSY signal of NXD1005/6. When the BUSY is Low, it means the internal FIFO buffer is full. If the BUSY(44QFP-#8, 24SOP-#7) pin is Low-level, this means that there is no space in internal FIFO buffer, therefore cannot access the data. Otherwise MCU stops the data writing for a while. If the BUSY is High-level, MCU can write the data to the NXD1005/6 for decoding.

In the I2C interface, SDA signal must be Low status during minimum 3us after Start signal for the stable operation.

Normal Operation

- Stand Alone

Without the microprocessor, NXD1005/6 can operate as “Stand Alone Operation” with key pad. Stand Alone Operation mode is judged internally without pin configuration.

- Designation of the Phrase for Decoding

When IKEYM(44QFP-#35) is High-level, it is possible to designate the phrase and sentence by using key0 ~ key11 directly. As IKEYM pin is Low-level, these keys are set with Matrix structure to designate 36 phrase or sentence. Also it can select phrase mode or sentence mode by setting SELSENT(44QFP-#15, 24SOP-#9) pin (0: Phrase mode, 1: Sentence mode).

When using the key switch, there is an electric and mechanical noise of the switch and this noise induce the malfunction. To prevent this, the key inputs are not accepted during 50ms after previous key inputs. Therefore the recommendation is to press the key over 200ms.

- Volume Control

The volume level can be changed by selecting the level of the VUP(44QFP-#1) and VDN(44QFP-#2) during the power on. When once pressing the VUP button, the 1dB level of volume increase from the initial volume you set. When once pressing the VDN button, the 1dB level will decrease. (Please refer to the volume chart - P.9)

- Repetition Play the Phrase

By pushing the RPT(44QFP-#43) pin`s switch, repetition play function is activated. Whenever this pin`s switch is pushed, the number of repetition is changed. (If this switch is pushed 4 times, the number of repetition is returned Once.)

Push Number	Repetition Number
0	1
1	2
2	4
3	Infinity

- Data Byte 0 Format(Header Code)

bit	[7:3]	[2]	[1:0]
name	Reserved	encode	Fs[1:0]

1) Fs[1:0] : sampling frequency. 2’b00:4khz, 2’b01:8khz, 2’b10:16khz
2) Encode : encoding of ADPCM. 1’b0:ADPCM, 1’b1:Not encoded
3) Data1 ~ Data N : Real Audio & Voice Data

Internal / External Memory Mode

- Internal Memory Mode

For the decoding the saved ADPCM data within the internal memory, Must come to be converted in proper format with Sampling Frequency 4/8/16KHz (8/16/32KHz). Also non-encoded data can be saved in the internal memory, but playing time is shorter than ADPCM data. After the setting other registers according to the necessity, the decode action will be processed with the selection of the designated phrase. By writing the designation number to Phrase Number Register, the decoding is started.

1) When user set the "0" to the Phrase Number Register, the first phrase is selected.

2) If the designated number is greater than the maximum number of recorded, the phrase that recorded last will be selected.

- External Memory Mode

The user can play the ADPCM or non-encoded data saved in the External Memory. It is available with controlling the register in NXD1005/6 by MCU. The format of ADPCM files which are stored in the external flash memory is compressed at 4 bit and sampling frequency 4/8/16kHz (8/16/32KHz) are possible. File conversion is a possibility of doing with NXD1005/NXD1006 PC program. The overall sequence is same as Play ADPCM Data. Also 16 bit PCM data must come to be converted with sameness rightly in NXD1005/NXD1006 formats. We recommend you use non-encoded data in direct play for a quality.

External memory can be used on only VDD 3.3V. The other power must be shifted the level to 3.3V.

Data Access to Internal Flash Memory

- Data Download Sequence

- Internal/external flash program mode setting(address E2h, data 01h)
- Flash Write protection clear operation(address 01h, data 00h)
- Flash chip erase operation(data C7h)
- Flash page program operation(Refer to figure3 on 12page.)
- Flash Write protection setting(address 01h, data 9Ch)
- Internal/external flash memory play mode setting(address E2h, data 00h)

- Write Enable (06h)

The Write Enable instruction (Figure 1) set the Write Enable Latch bit. The Write Enable Latch bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), and Write Status Register instruction.

The Write Enable instruction is entered by driving Chip Select (CSB) low, sending the instruction code, and then driving Chip Select (CSB) high.

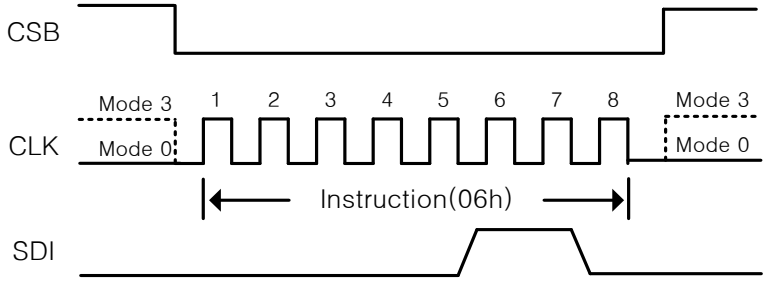


Figure 1. Write Enable instruction Sequence Diagram

- Write Status Register (01h)

The Write Status Register instruction allows new value to be written to the Status Register. Before it can be accepted, a Write Enable instruction must previously have been executed. After the Write Enable instruction has been decoded and executed, the device sets the Write Enable Latch.

The Write Status Register instruction is entered by driving Chip Select (CSB) low, followed by the instruction code and the data byte on Serial Data Input (SDI).

The instruction sequence is shown in Figure 2..

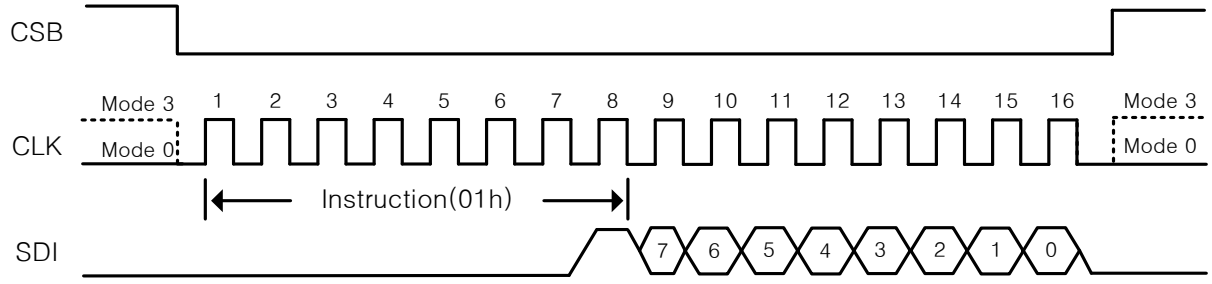


Figure 2. Write Status Register Instruction Sequence Diagram

- Page Program (PP) (02h)

The Page Program (PP) instruction allows bytes to be programmed in the memory. Before it can be accepted, a Write Enable instruction must previously have been executed. After the Write Enable instruction has been decoded, the device sets the Write Enable Latch.

The Page Program (PP) instruction is entered by driving Chip Select (CSB) low, followed by the instruction code, three address bytes and at least one data byte on Serial Data Input (SDI). If the 8 least significant address bits (A7 – A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page(from the address whose 8 least significant bits (A7 –A0) are all zero). Chip Select (CSB) must be driven low for the entire duration of the sequence.

The instruction sequence is shown in Figure 3. If more than 256bytes are sent to the device, previously latched data are discarded and the last 256 data bytes guaranteed to be programmed correctly within the same page. If less than 256 Data byte are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

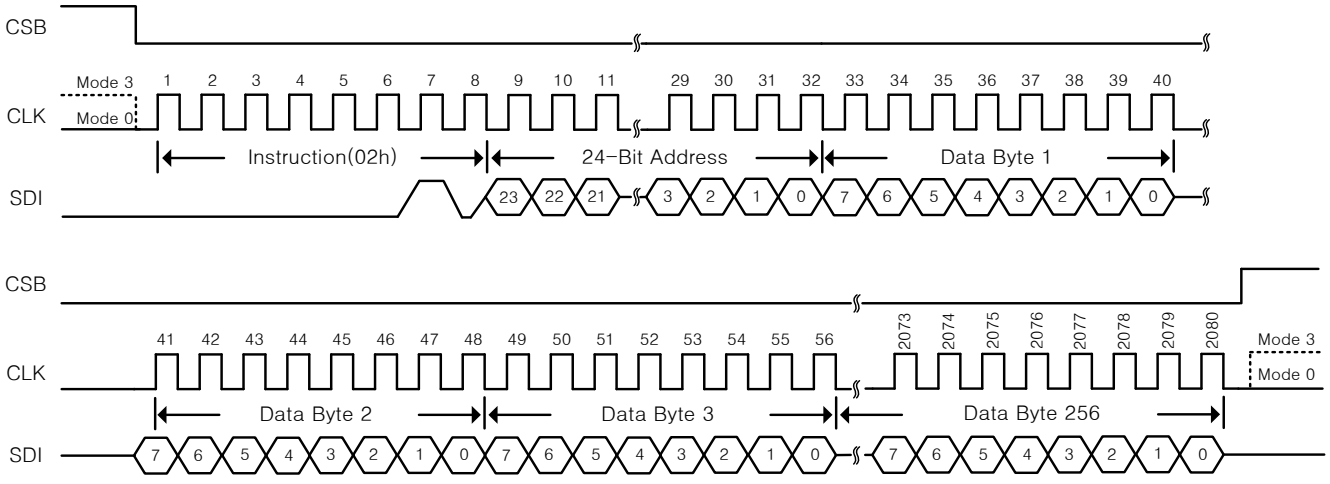


Figure 3. Page Program Instruction Sequence Diagram

- Sector Erase (SE) (20h)

The Sector Erase (SE) instruction sets to 1(FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable instruction must previously have been executed. After the Write Enable instruction has been decoded, the device sets the Write Enable latch.

The Sector Erase (SE) instruction is entered by driving Chip Selcet (CSB) low, followed by the instruction code, and three address bytes on Serial Data Input (SDI). The instruction sequence is shown in Figure 4.

Chip Select (CSB) must be driven high after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase (SE) is not executed.

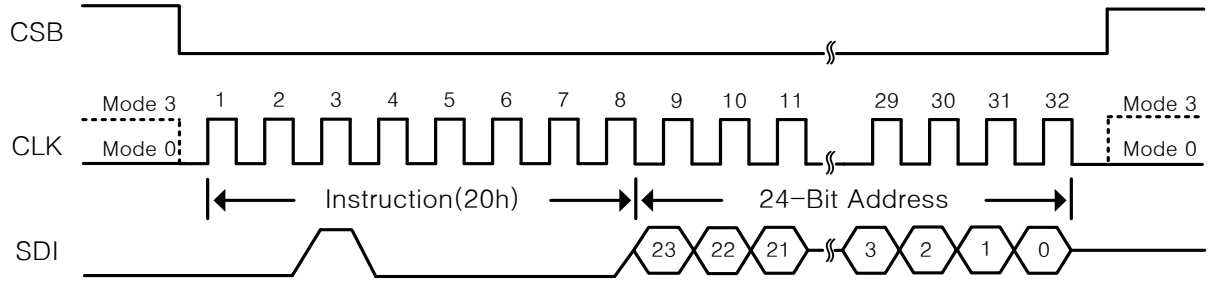


Figure 4. Sector Erase Instruction Sequence Diagram

- Block Erase (BE) (D8h)

The Block Erase (BE) instruction sets to 1 (FFh) all bits inside the chosen block. Before it can be accepted, a Write Enable instruction must previously have been executed. After the Write Enable instruction has been decoded, the device sets the Write Enable latch.

The Block Erase (BE) instruction is entered by driving Chip Select (CSB) low, followed by the instruction code, and three address bytes on Serial Data Input (SDI).

The instruction sequence is shown in Figure 5. Chip Select (CSB) must be driven high after the eighth bit of the last address byte has been latched in, otherwise the Block Erase (BE) is not executed.

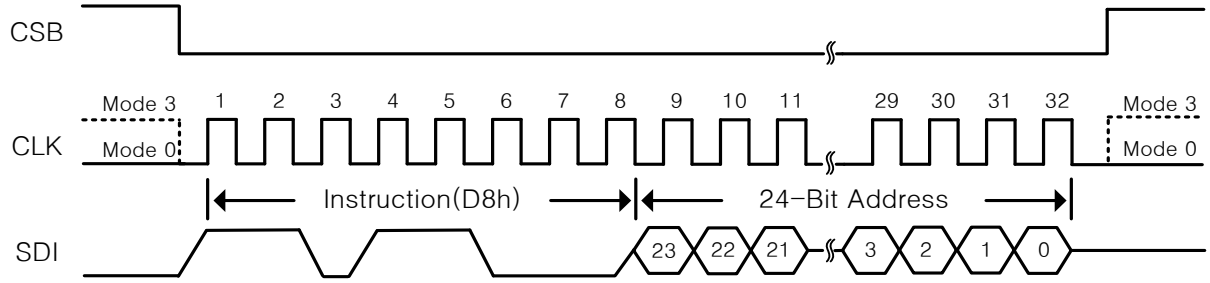


Figure 5. Block Erase Instruction Sequence Diagram

- Chip Erase(CE) (C7h)

The Chip Erase (CE) instruction sets all bits to 1(FFh). Before it can be accepted, a Write Enable instruction must previously have been executed. After the Write Enable instruction has been decoded, the device sets the Write Enable latch.

The Chip Erase (CE) instruction is entered by driving Chip Select (CSB) low, followed by the instruction code on Serial Data Input (SDI). Chip Select (CSB) must be driven low for the entire duration of the sequence.

The instruction sequence is shown Figure 6. Chip Select (CSB) must be driven high after the eighth bit of the instruction code has been latched in, otherwise the Chip Erase instruction is not executed.

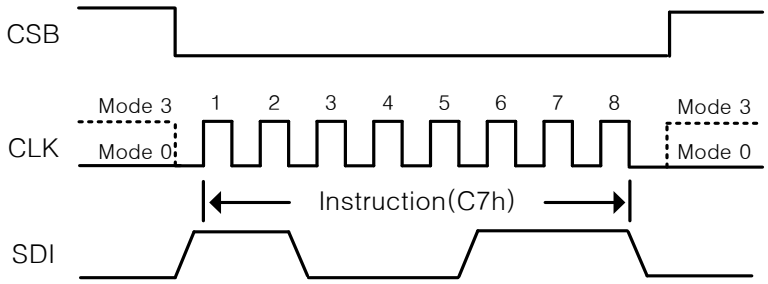


Figure 6. Chip Erase Instruction Sequence Diagram

Flash Memory Map

- Phrase Table (Address 0x000000 ~0x0017FF)

The Phrase Table is Pointer map concerning phrase audio data.
Phrase number is totally 255 from 0 to 254 and phrase number 255 is not available.
Phrase group number is totally 8 of 255 phrases
One Phrase is consist of 3 bytes (High byte, Middle byte, Low byte)
Phrase Table 0(Phrase group 1) is shown in Figure 1.

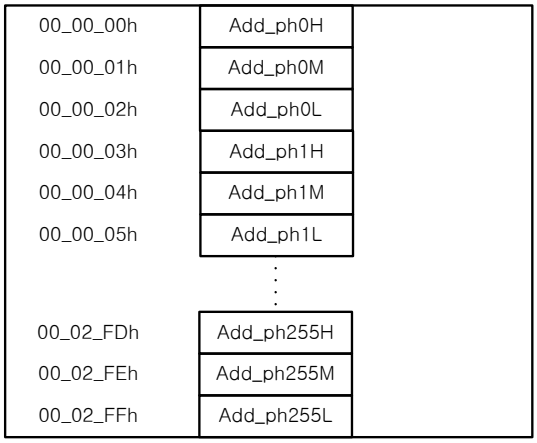


Figure 1. Phrase Table Diagram

- Sentence Table (Address 0x001800 ~0x0057FF)

The Sentence Table is capable to use maximum 8 phrases. If sentence use less than 8 phrases, you should program 0xFF behind the last phrase. You can use totally 2048 sentence number.
Sentence Table is shown in Figure 2.

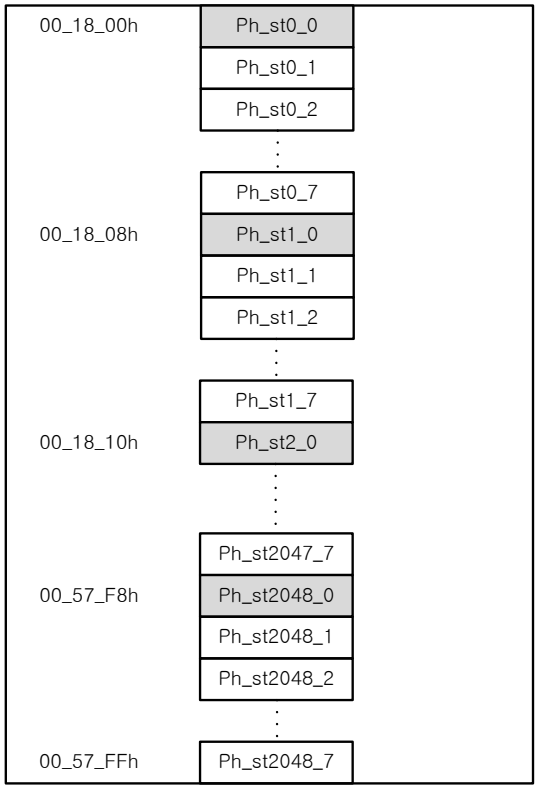
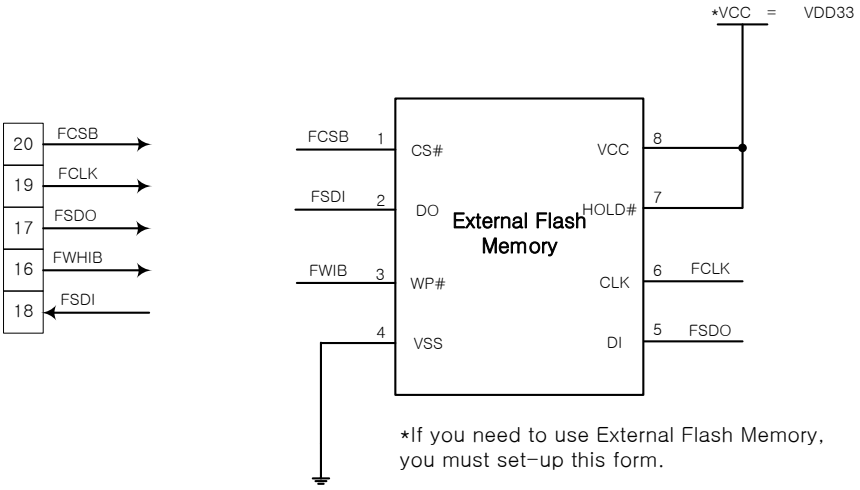


Figure 2. Sentence Table Diagram

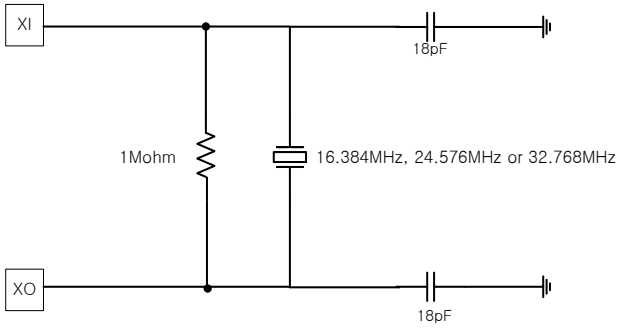
Application

- External Flash Memory SPI I/F Diagram



- X-tal usage recommendation

In case of using X-tal (We recommend that you should use this method as possible. It can play high quality of sound by using X-tal).

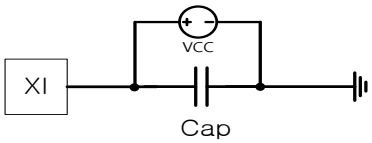


In case of using system clock (Recommended Frequency Fr = 16.384MHz, 24.576MHz or 32.768MHz),

System clock (16.384MHz, 24.576MHz or 32.768MHz)

* If clock is being used in the system, NXD1005/1006 can use this clock source directly with connecting to XI pin.

In case of using Resistor and Capacitor OSC built in (We do not recommend using RC OSC when you play high quality of sound),

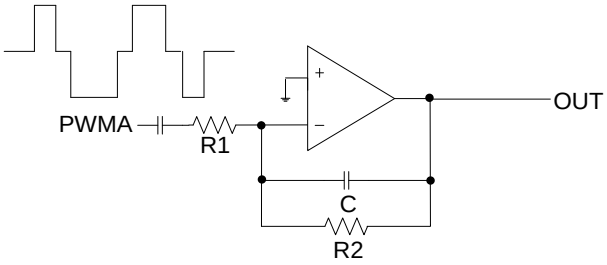


Cap

*Please connect XI input pin (#37-44QFP, #23-24SOP) to VCC.
Insert a capacitor(for eliminating noise) between XI and ground.
Capacitor size depend on the noise (We recommend 100nF).

- DA Application

DA Application



In DA Application, when DA pin (44QFP-#21) is "Low Level", it operates in normal mode.
When DA pin is "High Level", loop gain is set through R1 and R2 and the frequency of LPF is set through C.

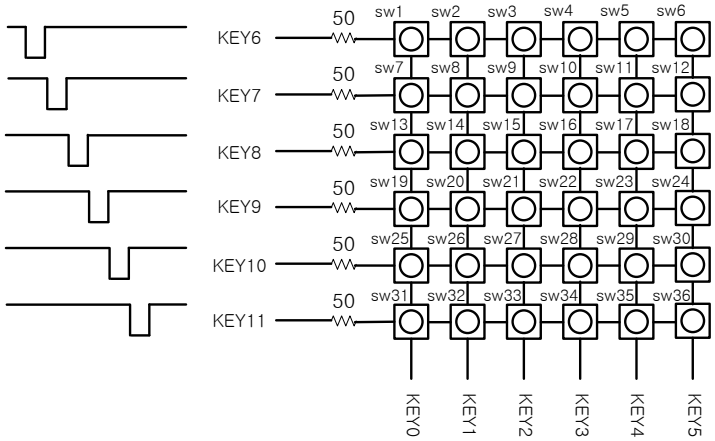
$$\text{Gain} = \frac{R2}{R1} \qquad f_{lpf} = \frac{1}{2\pi R2C}$$

We recommend that R1,R2 ≒ 4.7kohm, C ≒ 1.5nF

- Play Monitor Option

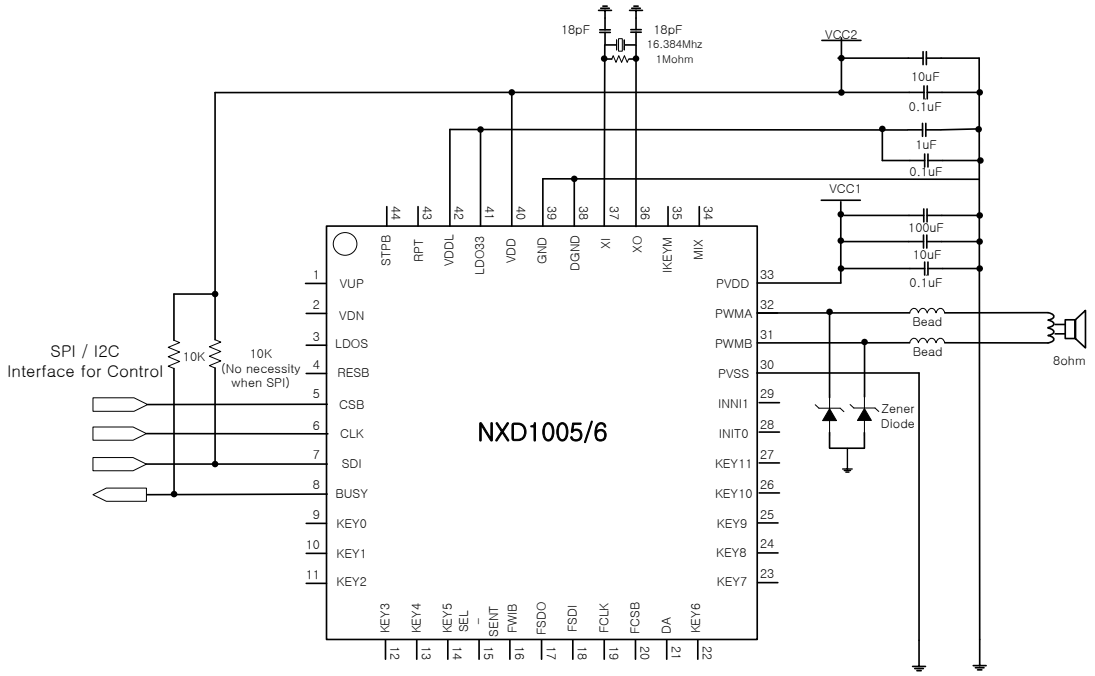
It is available to check playing status with Play Monitor Option.
Address E3h, data 05h : Play Monitor Enable, data 00h : Play Monitor Disable.
Address E2h, data 60h : Play Signal Monitor Pin Mapping.
It can check playing status through Pin KEY11 (44QFP-#27, 24SOP-#15).
KEY11 is "High" while playing and KEY11 is "Low" when stop playing.
In Play Monitor Option, Pin INIT0(44QFP-#28, 24SOP-#16) and INIT1(44QFP-#29, 24SOP-#17) are Output pins. In the case that these pins are connected to VCC, GND or u-com output, insert the 5K resistors to input stage of these pins for prevention the unwanted current.

- Matrix Method Diagram



In operation mode, Output keys (key6 ~ key11) outputs signals such an above diagram. Namely, when output key`s status is low level, NXD1005/6 can detect the status of input keys (key0 ~key5).

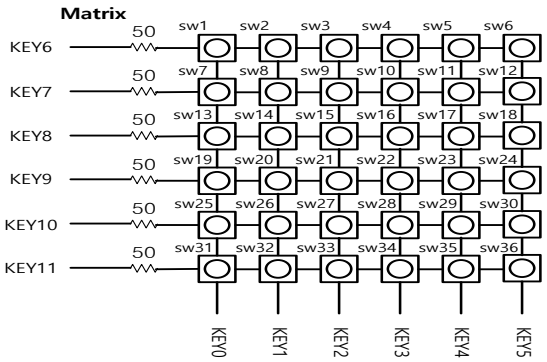
- Stand Alone application

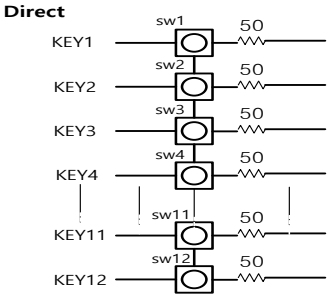


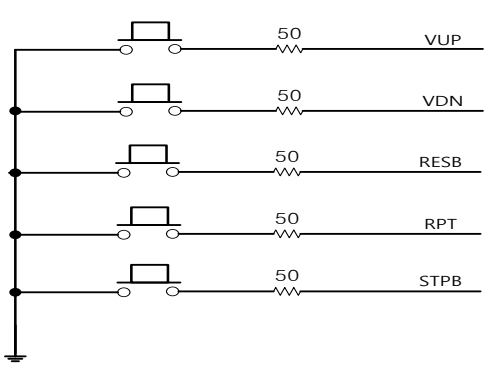
※Recommendation : Zener Diode -1N5231B, Bead - EBMS201209B202

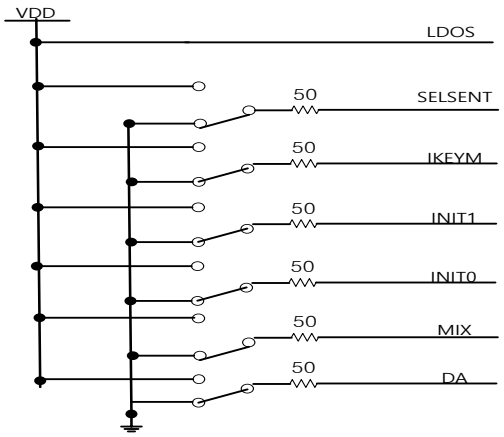
※PVDD Cap must be attached with in 10mm.

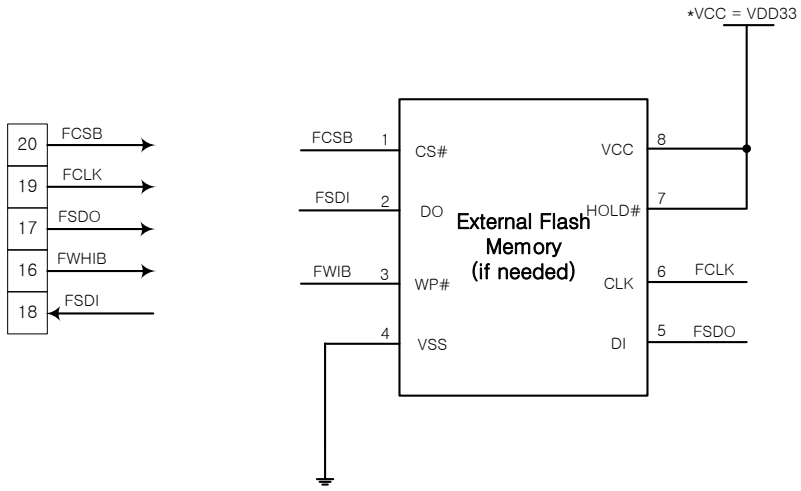
VCC1 and VCC2 are same voltage but It should be separated to avoid reset event.
If it is connected directly between VDD (44QFP-#40) and PVDD (44QFP-#33), there is a possibility to be reset because current consumption of PVDD is very much. So we recommend that Power line is separated in drawing PCB.











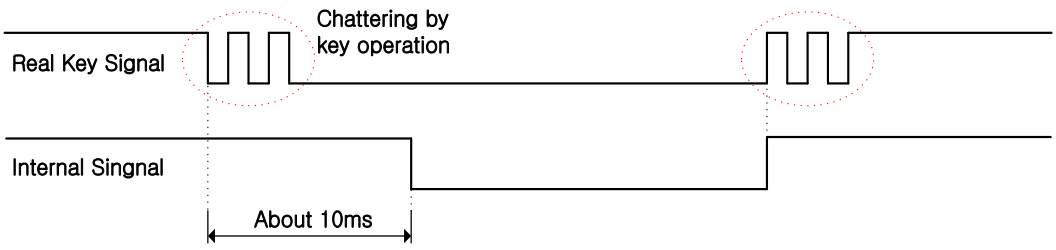
From Stand Alone Operation, the decoding is accomplished key switch. If IKEYM (44QFP-#35) is Low-level, NXD1005/1006 is equipped with 6 input keys (key0 ~ key5) and 6 output keys (key6 ~ key11). It can designate 36 phrases (6X6 - matrix) with time sharing by output keys. When IKEYM is High-level, NXD1005/6 is equipped with 12 input keys (key0 ~ key11). It can designate 12 phrases (direct) - ex>phrase1 apply to input key1, phrase 2 apply to input key 2. Also it is equipped with volume control pins (VDN and VUP). When VDN key is pressed one time, the volume decreases 1dB. When VUP key is pressed once, the volume will increase 1dB. Initial Volume is set with INIT0 and INIT1 pin at the power-on time. After power-on, these pin`s status does not affect to the volume level but it must be fixed in flash programmable mode.

It is enable to play for repetition by setting RPT pin`s switch. Whenever this pin`s switch is pushed, the number of repetition is changed.(If this switch is pushed 4 times, repetition number is returned once.)

STPB controls stop function during the playing phrase. This action is operated with setting one`s status "Low".

From Stand Alone Operation, when the decoding action for the selected file is completed, NXD1005/6 goes to the clock stop mode. If the one of key(key0 ~ key11) is pressed, the internal clock wake and then operate.

- Key Operation in Standalone Mode

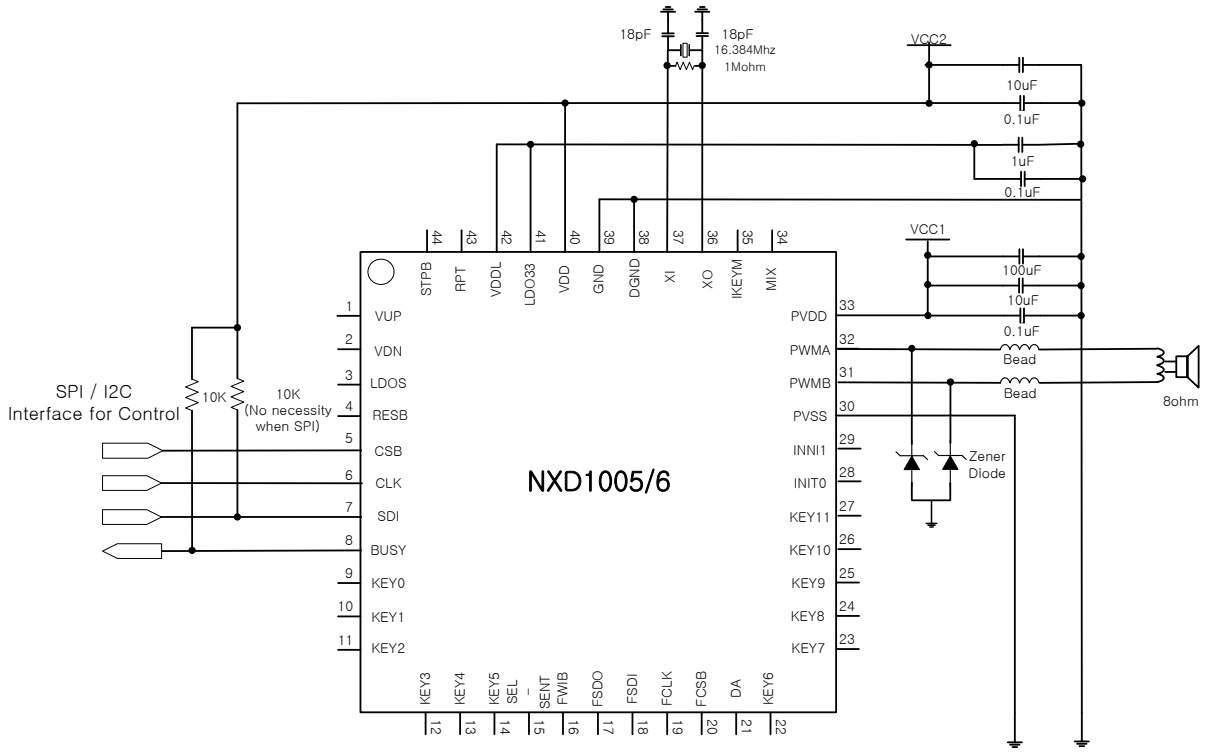


When using the key switch, there is an electric and mechanical noise of the switch such an above diagram and this noise induces the malfunction.

To prevent this malfunction, NXD1005/1006 outputs Internal Signal delayed 10ms from key operation. When key operation is ended, Internal Signal is change to "High" right.

- MCU application

- 44Pin QFP



※Recommendation : Zener Diode -1N5231B, Bead - EBMS201209B202

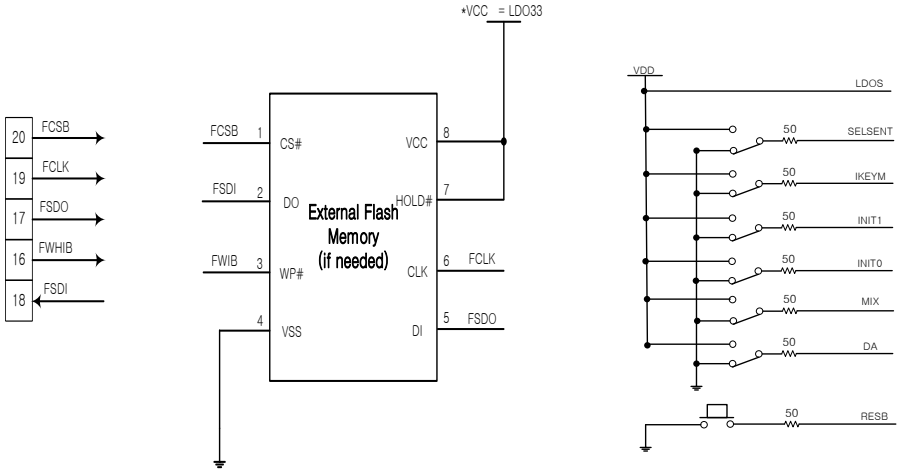
※PVDD Cap must be attached with in 10mm.

※Caution

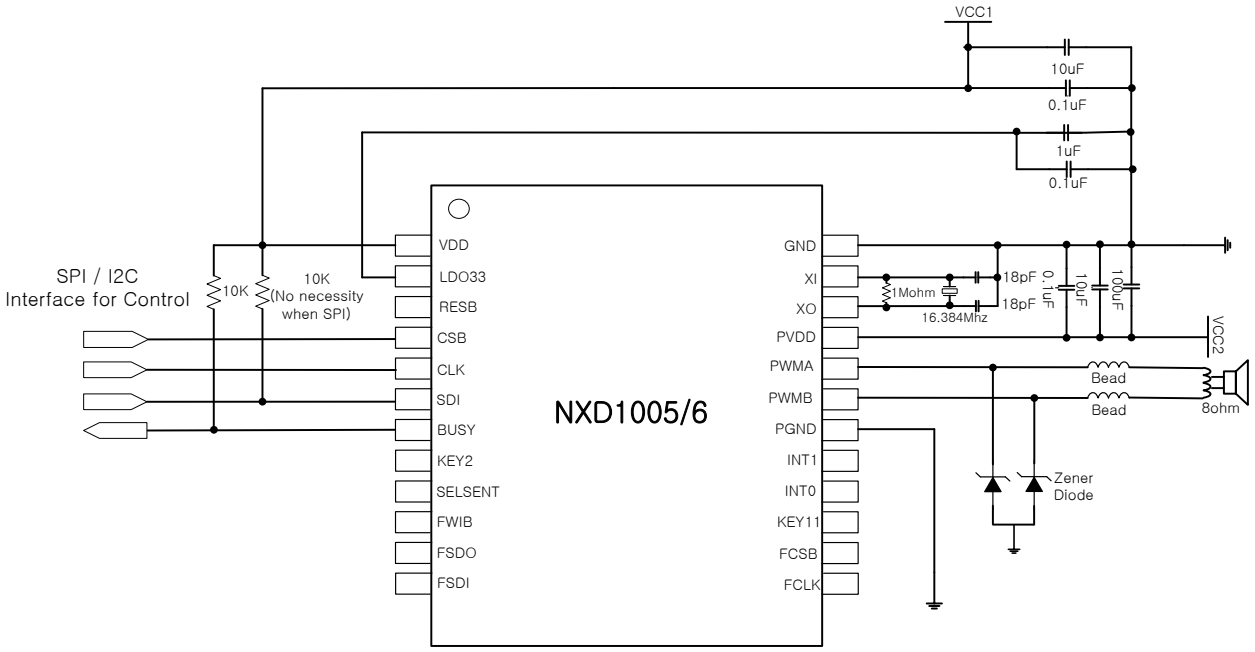
There is no need the pull-up resistor for KEY0~KEY5 pin.
Because NXD1005/1006 has internally pull-up for these, if you connect to ground (GND), the unwanted current flows and increases the power consumption.

If you want to play phrase and sentence by turns, MCU should control SELSENT (#15). If the status of SELSENT is changed, it is applied from next turn.
You should monitor LDO33 (#41) pin to confirm playing status.

In case of External flash application, you should connect flash's VCC to LDO33.
Internal LDO is enough to drive flash memory, also you should connect LDO33.



- 24Pin SOP



※Recommendation : Zener Diode -1N5231B, Bead - EBMS201209B202

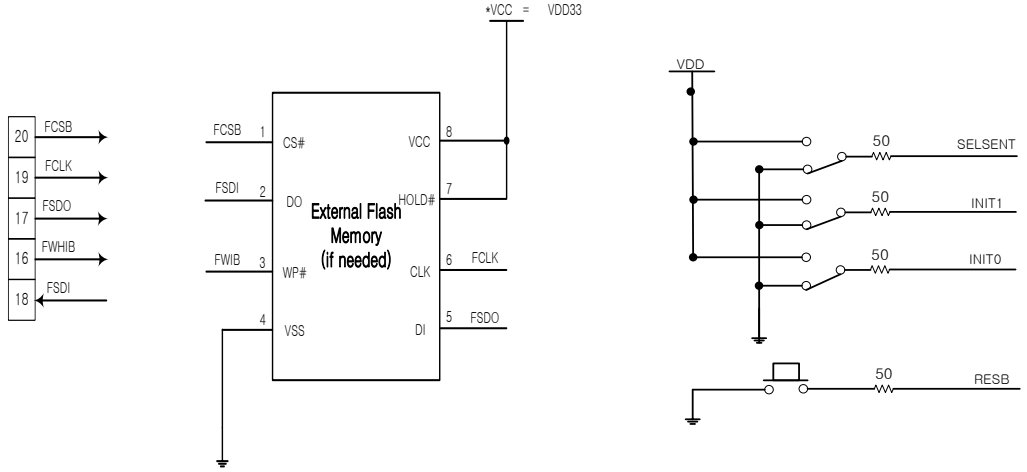
※PVDD Cap must be attached with in 10mm.

※Caution

There is no need the pull-up resistor for KEY2 and KEY11 pin.
Because NXD1005/1006 has internally pull-up for these, if you connect to ground (GND), the unwanted current flows and increases the power consumption.

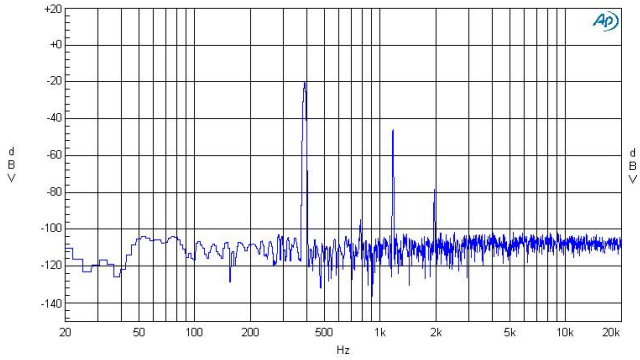
If you want to play phrase and sentence by turns, MCU should control SELSENT (#9). If the status of SELSENT is changed, it is applied from next turn.
You should monitor LDO33 (#2) pin to confirm playing status.

In case of External flash application, you should connect flash's VCC to LDO33.
Internal LDO is enough to drive flash memory, also you should connect LDO33.

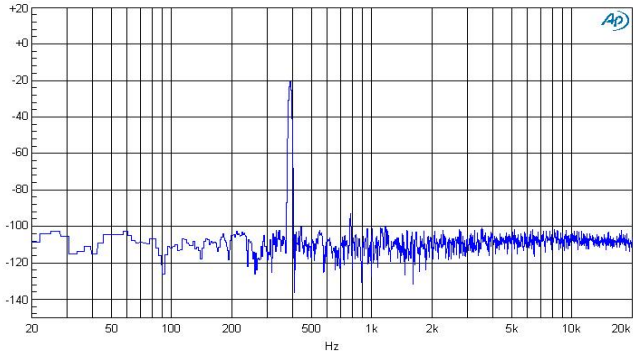


FFT Waveform

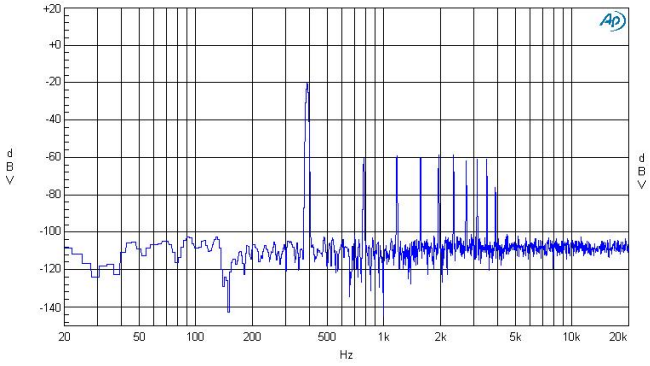
- Gain (-20dB) , Sine Wave(400Hz)



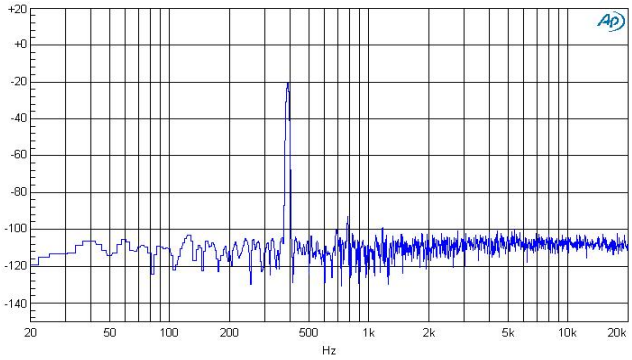
4KHz(ADPCM)



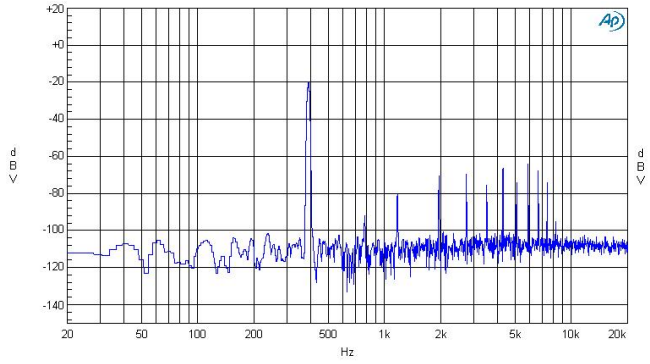
4KHz(Linear)



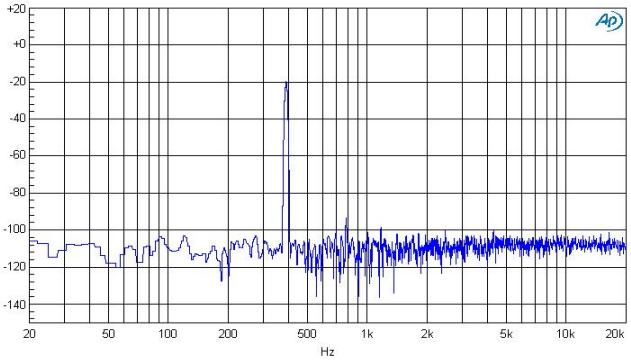
8KHz(ADPCM)



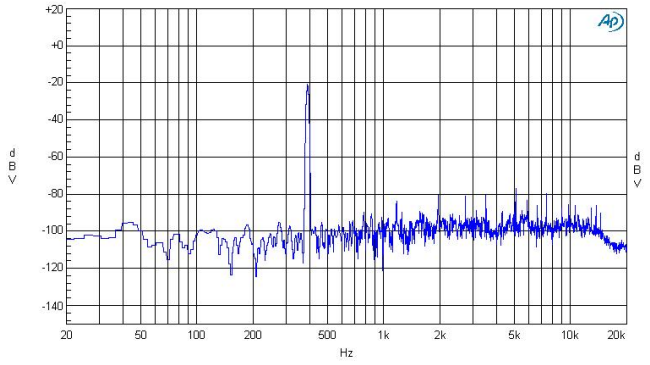
8KHz(Linear)



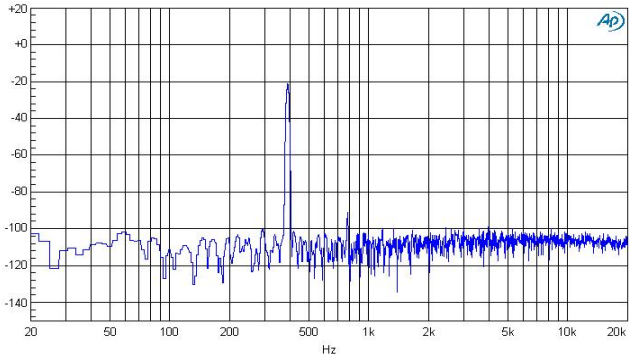
16KHz(ADPCM)



16KHz(Linear)

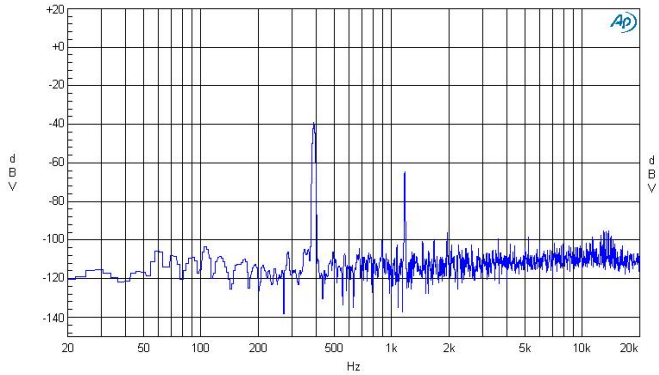


32KHz(ADPCM)

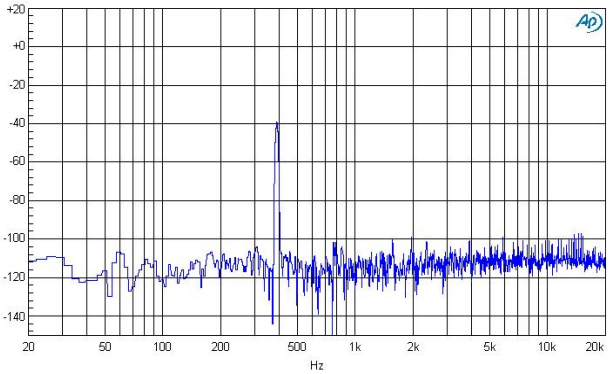


32KHz(Linear)

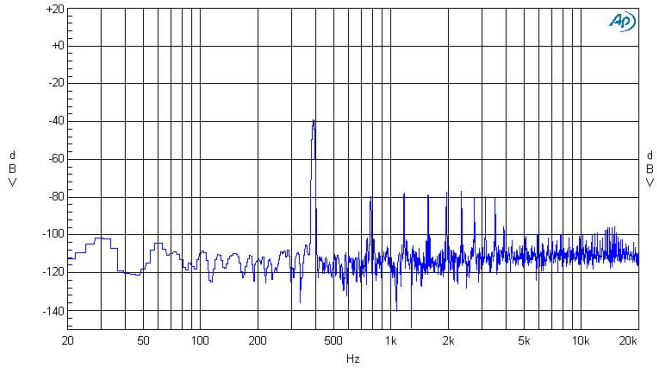
- Gain (-40dB) , Sine Wave(400Hz)



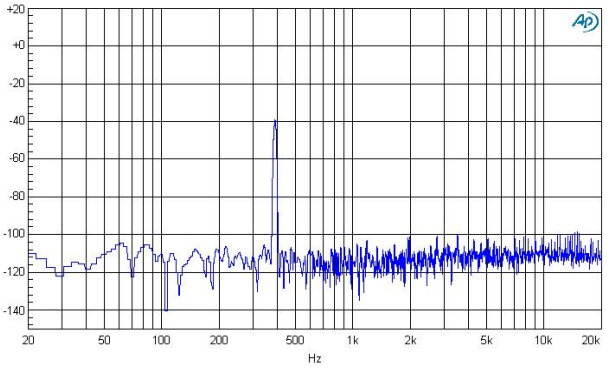
4KHz(ADPCM)



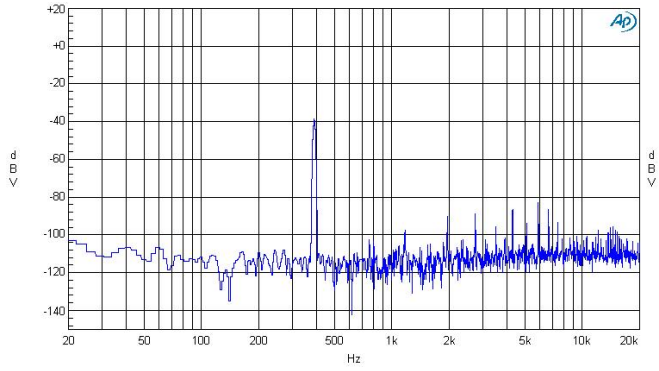
4KHz(Linear)



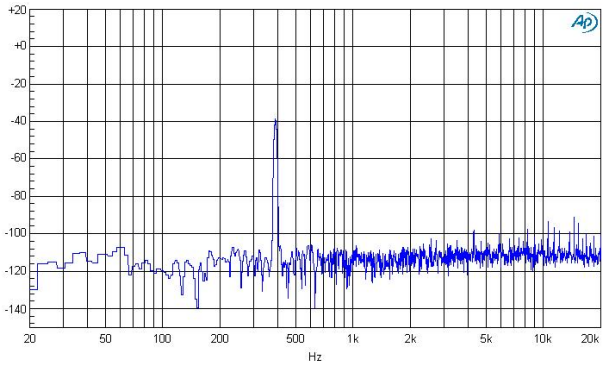
8KHz(ADPCM)



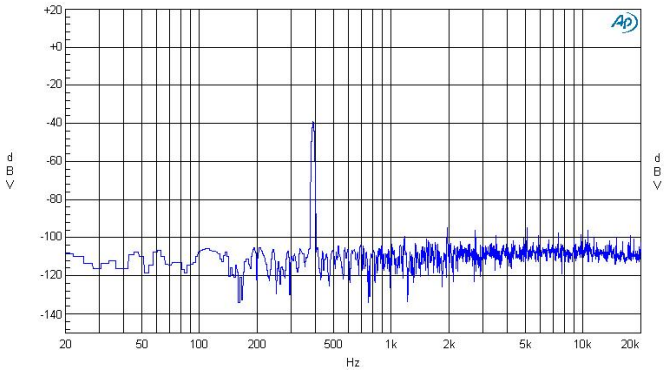
8KHz(Linear)



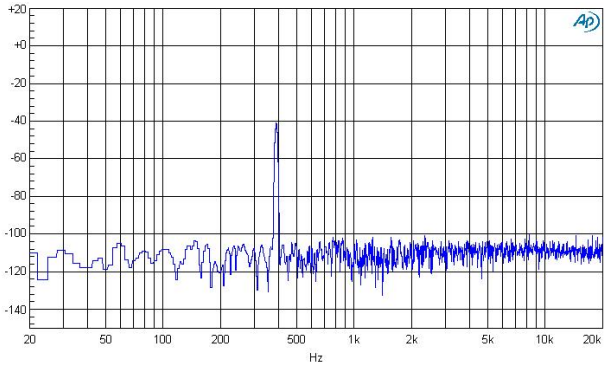
16KHz(ADPCM)



16KHz(Linear)

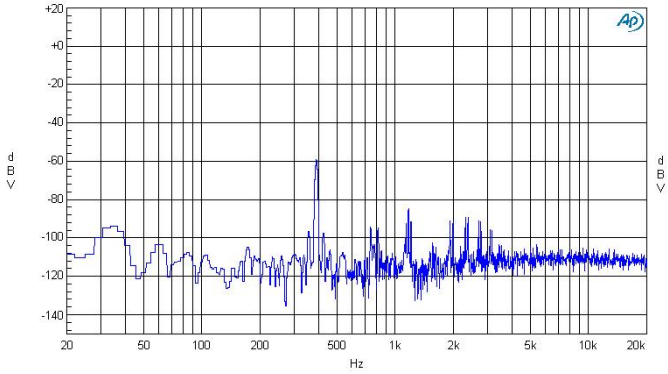


32KHz(ADPCM)

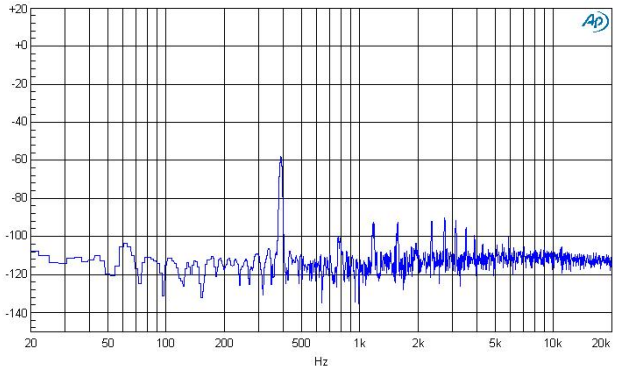


32KHz(Linear)

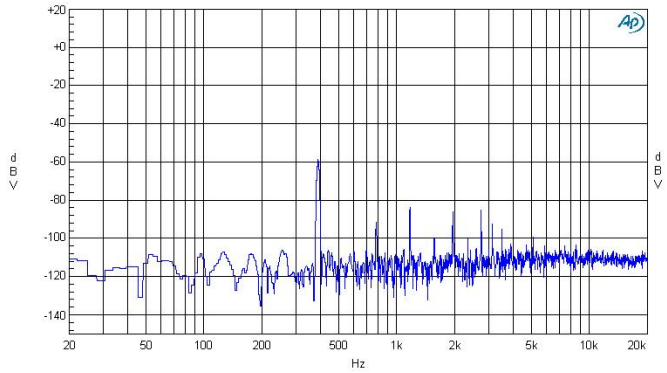
- Gain (-60dB) , Sine Wave(400Hz)



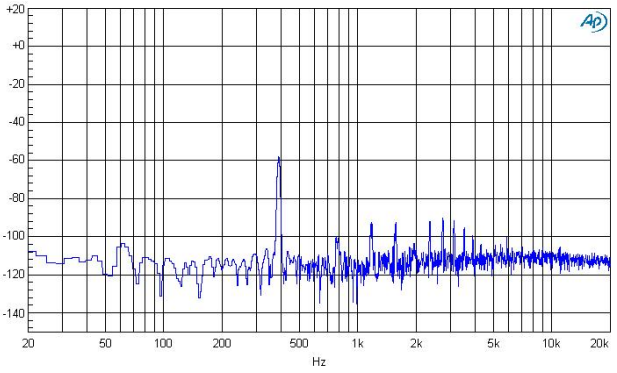
4KHz(ADPCM)



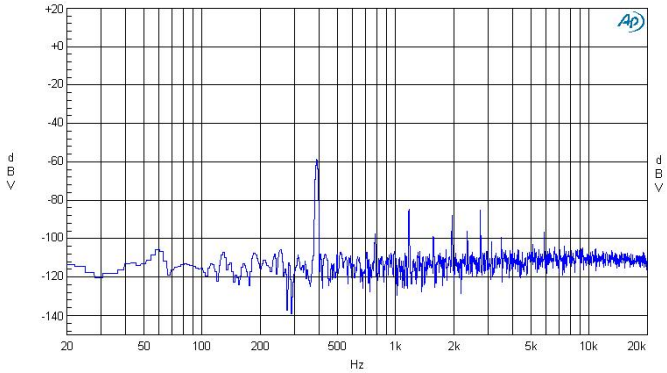
4KHz(Linear)



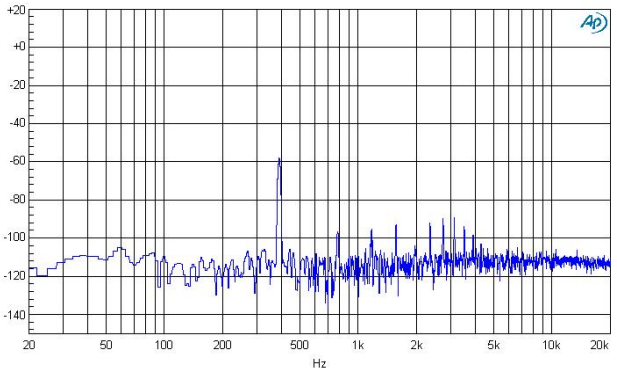
8KHz(ADPCM)



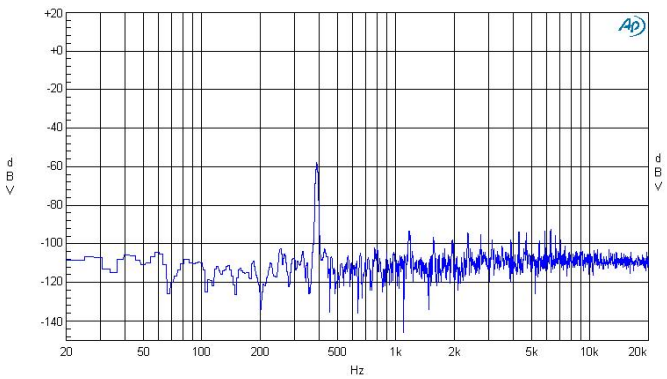
8KHz(Linear)



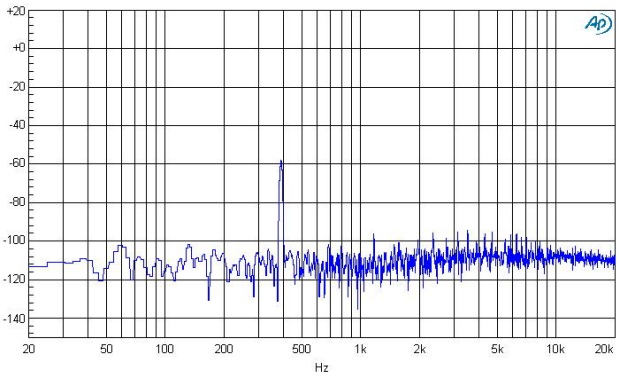
16KHz(ADPCM)



16KHz(Linear)

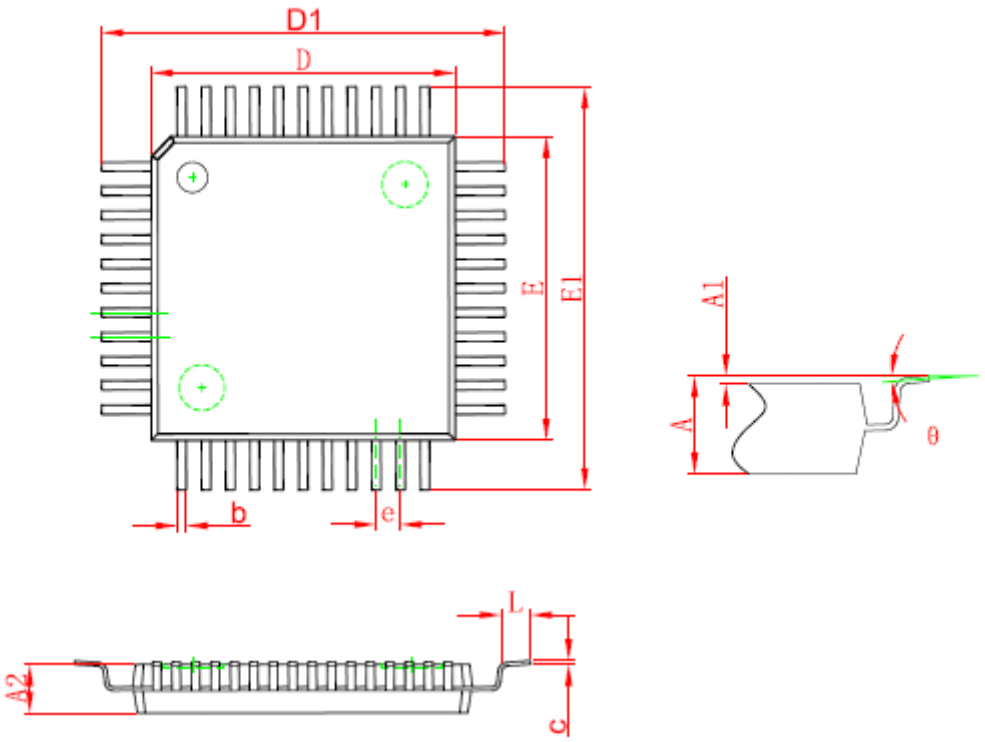


32KHz(ADPCM)



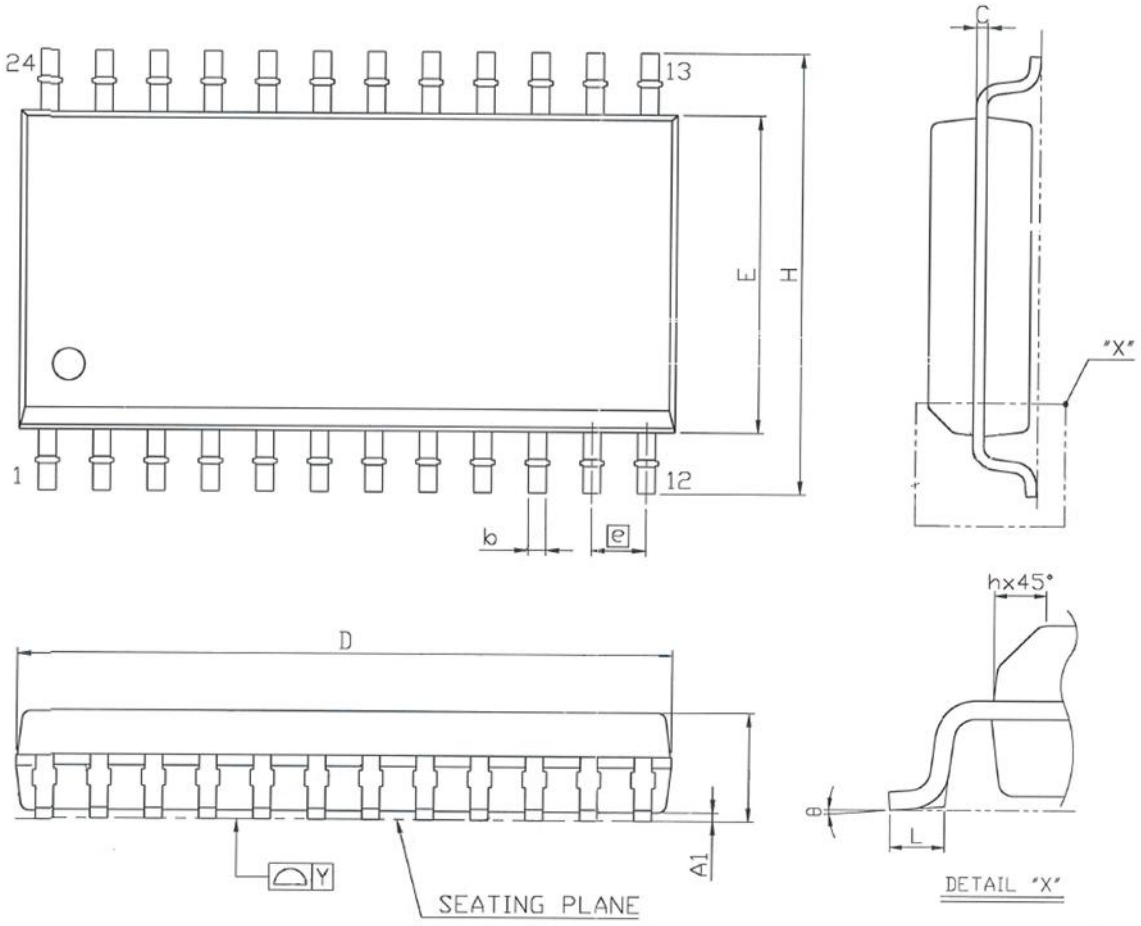
32KHz(Linear)

Package Dimensions (44QFP)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.600		0.063
A1	0.050	0.150	0.002	0.006
A2	1.350	1.450	0.053	0.057
b	0.280	0.400	0.011	0.016
c	0.100	0.200	0.004	0.008
D	9.900	10.100	0.390	0.398
D1	11.850	12.150	0.467	0.478
E	9.900	10.100	0.390	0.398
E1	11.850	12.150	0.467	0.478
e	0.800 (BSC)		0.031 (BSC)	
L	0.450	0.750	0.018	0.030
θ	0°	7°	0°	7°

Package Dimensions (24SOP)



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2,36	2,54	2,64	93	100	104
A1	0,10	0,20	0,30	4	8	12
b	0,35	0,406	0,48	14	16	19
c	0,23	0,254	0,31	9	10	12
D	15,20	15,29	15,60	598	602	614
E	7,40	7,50	7,60	291	295	299
e	1,27 BSC			50 BSC		
H	10,00	10,31	10,65	394	406	419
h	0,25	0,66	0,75	10	26	30
L	0,51	0,76	1,02	20	30	40
Y			0,075			3
θ	0°		8°	0°		8°