NXD1003A/1004A

Voice Player with Digital Amplifier & 8M Flash

General Description

The NXD1003A/1004A is an ADPCM codec Voice player.
It includes Digital amplifier and enable to drive 6～16 ohm speaker directly.
The NXD1003A is a non flash memory version and the NXD1004A is a embedded 8M flash memory version.
And all of them can extend external flash memory.
The NXD1003A/1004A can be used Stand alone mode or u-Com mode.

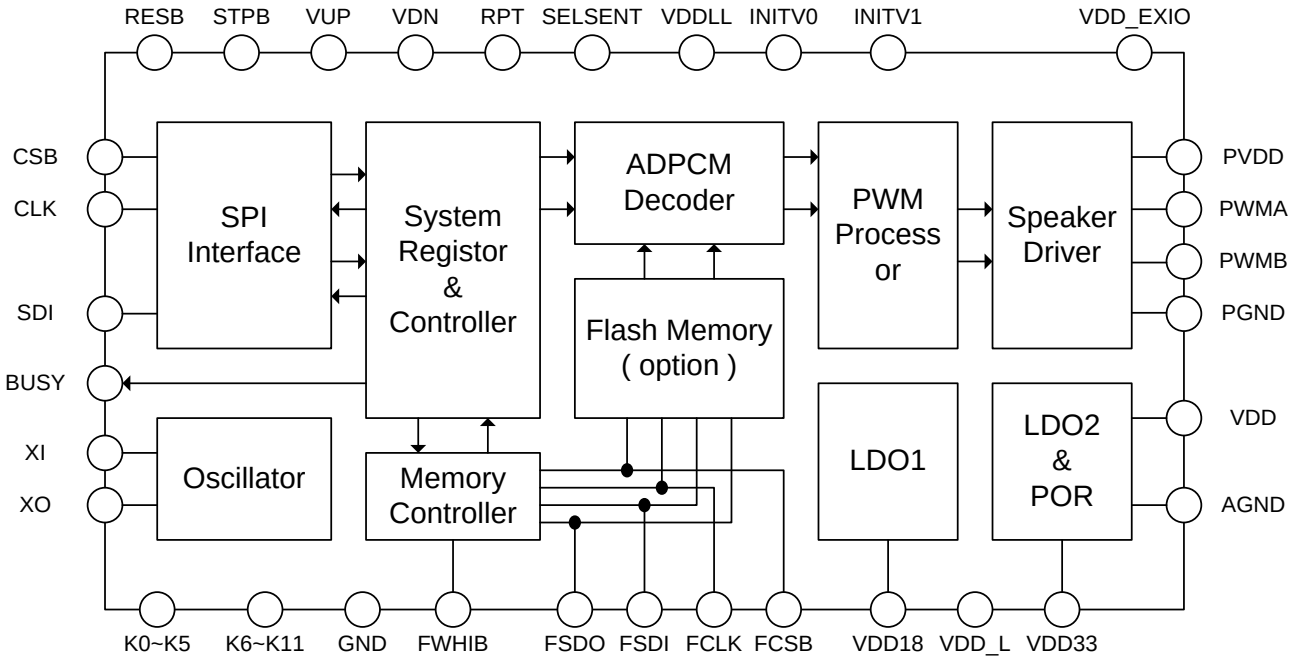
Feature

- Supply voltage : 2.8V ~ 5.5V
- 16bits operation in ADPCM Decoder
- Stand alone / SPI control interface
- Program play : Selectable Phrase play or Sentence play
- Direct play : PCM or ADPCM input
- Non-Encoded data can be saved in the Internal/external flash memory for high quality.
- Direct internal/external serial flash memory access
- Direct speaker drive with internal Digital amplifier
  600mW @ 8ohm, THD=10% (VCC=3.3V)
  1.5W @ 8ohm, THD=10% (VCC=5.5V)
- X-tal oscillator or Passive ring oscillator : Master clock Frequency is 16.384 or 32.768MHz
- Maximum 36 keys(matrix structure) at stand alone mode
- Auto power save mode for very long battery life time
- Sampling rate : 4, 8, 16KHz / 8, 16, 32KHz(X-tal : 16.384MHz / 32.768MHz)
- Maximum play time (@ internal 8M, 4K Sampling rate) : 500sec
- Built in 2 Low Dropout Regulators for internal/external flash or u-com
- Built in Power on reset
- Auto stand-by : under 0.1uA when no key action
- A few external parts
- Package : 36SSOP, 44QFP, 48QFN
-

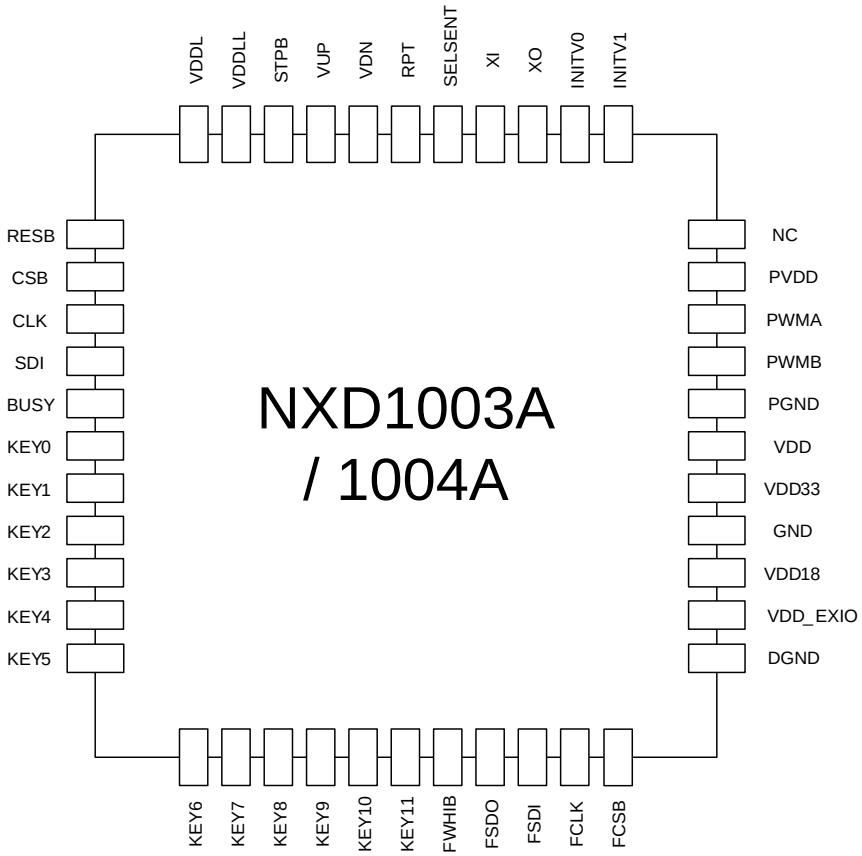
Application

- Toys
- GPS, Navigation
- Audio book
- Answering machine
- Home voice applications

Block Diagram



Terminal assignment (44QFP)



Pin description (44QFP)

Pin Name	No.	I/O	Description	Act.	PU/PD
RESB	1	I	Power On Reset pin	L	PU
CSB	2	I	SPI enable pin (If EnPgm(E4h[7])is H, It is CSB of Internal Flash)	L	PU
CLK	3	I	SPI clock (If EnPgm(E4h[7])is H, It is CK of Internal Flash)	–	–
SDI	4	I	SPI Data input (If EnPgm(E4h[7])is H, It is DI of Internal Flash)	–	–
BUSY	5	O	SPI BUSY signal (If EnPgm(E4h[7])is H, It is DO of Internal Flash)	L	–
KEY0	6	I	Input key0 for selecting phrase	L	PU
KEY1	7	I	Input key1 for selecting phrase	L	PU
KEY2	8	I	Input key2 for selecting phrase	L	PU
KEY3	9	I	Input key3 for selecting phrase	L	PU
KEY4	10	I	Input key4 for selecting phrase	L	PU
KEY5	11	I	Input key5 for selecting phrase	L	PU
KEY6	12	O	Output key6 for selecting phrase	–	–
KEY7	13	O	Output key7 for selecting phrase	–	–
KEY8	14	O	Output key8 for selecting phrase	–	–
KEY9	15	O	Output key9 for selecting phrase	–	–
KEY10	16	O	Output key10 for selecting phrase	–	–
KEY11	17	O	Output key11 for selecting phrase /Playing Status Monitor Pin	–	–
FWHIB	18	O	write inhibit output of the external flash memory	L	–
FSDO	19	O	Serial data input of the external flash memory	–	–
FSDI	20	I	Serial data output of the external flash memory	–	PD
FCLK	21	O	Clock input Of the External flash memory	–	–
FCSB	22	O	Chip select signal Of the External flash memory	L	–
DGND	23	G	Digital ground	–	–
VDD_EXIO	24	P	Power selection pin Of the External flash memory	–	–
VDD18	25	O	LDO 1.8V output	–	–
GNDA	26	G	Analog ground	–	–
VDD33	27	O	LDO 3.3V output	–	–
VDD	28	P	VDD (for LDO)	–	–
PGND	29	G	Power ground	–	–
PWMB	30	O	Amplifier out B	–	–
PWMA	31	O	Amplifier out A	–	–
PVDD	32	P	Power VDD	–	–
NC	33	–	Not Connected	–	–
INITV1	34	I/O	Initial volume setting pin 1	–	–
INITV0	35	I/O	Initial volume setting pin 0	–	–
XO	36	O	X-tal oscillator output	–	–

XI	37	I	X-tal oscillator input	-	-
SELSENT	38	I	Play mode selection pin (0:phrase 1:sentence)	-	-
RPT	39	I	Repeat circulation in phrase mode	L	PU
VDN	40	I	Volume down pin (for Stand alone)	L	PU
VUP	41	I	Volume up pin (for Stand alone)	L	PU
STPB	42	I	Play stop control pin	L	PU
VDDLL	43	P	Enable to supply 1.8V to internal flash memory.	-	-
VDDL	44	I	Digital power (Must be connected to VDD33)	-	-

Maximum Absolute ratings

Parameter	Symbol	Value	Unit
Supply Voltage	Vccmax	-0.3 ~ 6.0	V
Storage temperature	Tstg	-45 ~ 150	℃
Operating temperature	Topr	-40 ~ 85	℃
Power Dissipation	Pdmax	800	mW

ESD Characteristics

Mode	Polarity	Characteristic			Unit
		min	typ	max	
HBM	Positive/Negative	2000	-	-	V
MM	Positive/Negative	200	-	-	V
CDM	Positive/Negative	800	-	-	V

Electrical Characteristics

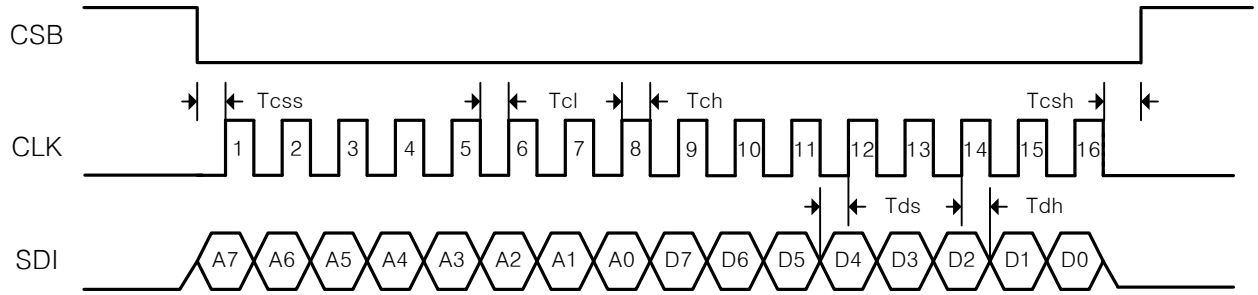
VCC = 5.0V, Ta=25.0℃ Unless otherwise noted

Characteristics	Symbo	Condition	Value			Unit
			min	typ	max	
Operating voltage range	Vop	-	2.8	-	5.5	V
Stand by current	Ist	Vin=5.0V	-	0.0	1.0	uA
Shut down current	Isd	Vin=5.0V	-	0.0	1.0	uA
Output Power	Po	8ohm, 10%, VIN=3.3V	500	600	-	mW
LDO1 output voltage	Vout1	Vin=5.0V	1.5	1.8	2.1	V
LDO2 output voltage	Vout2	Vin=5.0V	3.0	3.3	3.6	V
Total harmonic distortion + N	THD+N	8ohm, Po=40mW, 1KHz	-	0.1	-	%
Volume control range	Rvol	-	-98	-	+24	dB
Initial Setting Time(*)	T_{INIT}	-		250	500	ms

* After NXD1003/4A is reset or power on, you should wait for Initial Setting Time.
Initial Setting Time is for reading internal flash information and setting initial volume.

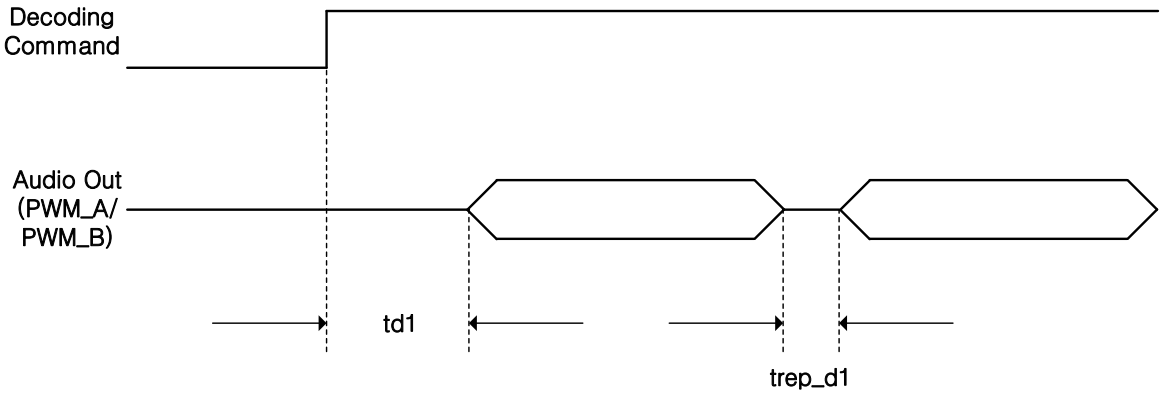
Timing Diagram

- SPI Timing (CSB, CLK, SDI)



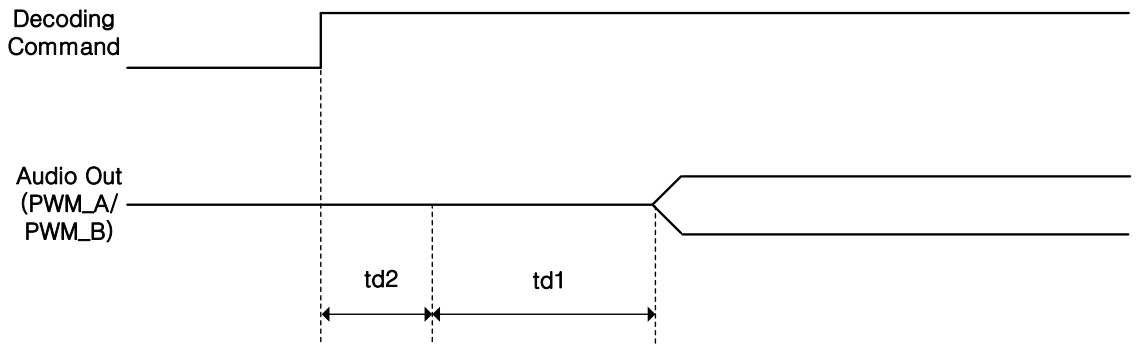
Parameter	Symbol	2.7 ~ 4.4V	4.5 ~ 5.5V	Unit
Clock Width High	Tch	500	400	ns min
Clock Width Low	Tcl	500	400	ns min
Data Setup	Tds	100	80	ns min
Data Hold	Tdh	60	50	ns min
Select	Tcss	60	50	ns min
Deselect	Tcsh	120	100	ns min

- Decode timing (Using internal flash memory mode)



The td1 is the time-gap between the stat command for decode and the real audio output.

- Decode timing (Using external flash memory mode)



Parameter	Symbol	fs=4KHz	fs=8KHz	fs=16KHz	comments
Data out delay	td1	32ms	16ms	8ms	-
FIFO buffer delay	td2	-	-	-	*1
Blank period in repeat mode	trep_d1	16ms	8ms	4ms	repeat mode

*1 : The td2 is the data downloading time from the External Memory to FIFO buffer.
NXD1004A has the 256 byte FIFO for the data buffer.

Sampling Rate

NXD1003A/1004A can play non-encoded or encoded data(ADPCM). NXD1003A/1004A supplies normally 4,8,16KHz sampling rate by using 16.384MHz in system clock. Also NXD1003A/1004A supports 8,16,32KHz in the option. You should use 32.768MHz in system clock for 8,16,32KHz sampling rate. In case that you use 32KHz sampling rate, we recommend non-encoded data for much better sound quality. Because non-encoded is fewer noise than encoded data(ADPCM).

Register Map

Name	Addr	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
Phrase Number1	$E0h	0~254 Phrase / Sentence[7:0]								0x00
Volume	$E1h	Volume (+24~-96dB)								0x24
Control0	$E2h	-			Stop	Repeat[1:0]		OprMode[1:0]		0x00
Control1	$E3h	EnDth	SymDth	AmtDth[1:0]		EnFlt	-			0x00
Phrase Number2	$E4h	EnPgm	-	Phrase Group[2:0]			Sentence[10:8]			0x00

- Phrase Number Register ($E0h & $E4h)

This register designates the phrase number or sentence number for decoding.
There are 8th group of 255phrases. You can select phrase group by setting $E4h register.
There are 2048 sentences that are combined with 8 phrases.
You can play voice and music by setting $E0h register.

- Volume Control Register ($E1h)

This register controls the volume of the signal.

Number	Volume[dB]	Number	Volume[dB]	Number	Volume[dB]	Number	Volume[dB]
00h	+24	01h	+23	02h	+22	03h	+21
04h	+20	05h	+19	06h	+18	07h	+17
08h	+16	09h	+15	0ah	+14	0bh	+13
0ch	+12	0dh	+11	0eh	+10	0fh	+9
10h	+8	11h	+7	12h	+6	13h	+5
14h	+4	15h	+3	16h	+2	17h	+1
18h	0	19h	-1	1ah	-2	1bh	-3
1ch	-4	1dh	-5	1eh	-6	1fh	-7
20h	-8	21h	-9	22h	-10	23h	-11
24h	-12	25h	-13	26h	-14	27h	-15
28h	-16	29h	-17	2ah	-18	2bh	-19
2ch	-20	2dh	-21	2eh	-22	2fh	-23
30h	-24	31h	-25	32h	-26	33h	-27
34h	-28	35h	-29	36h	-30	37h	-31
38h	-32	39h	-33	3ah	-34	3bh	-35
3ch	-36	3dh	-37	3eh	-38	3fh	-39
40h	-40	41h	-41	42h	-42	43h	-43
44h	-44	45h	-45	46h	-46	47h	-47
48h	-48	49h	-49	4ah	-50	4bh	-52
4ch	-54	4dh	-56	4eh	-58	4fh	-60
50h	-64	51h	-68	52h	-72	53h	-78
54h	-84	55h	-90	56h	-96	57h	-98

- Control0 Register ($E2h)

OprMode (Operating Mode) :
You can select operating Mode by setting these two bits.

0h : Nomal Play from Internal/External flash memory.
1h : Internal/External Flash Memory Program Mode.
2h : Direct Play Mode (etc. : PC control program)

Repeat :
This two bits register is for the repetition play for the selected phrase or sentence.
0h : 1-time play 1h : 2-time play
2h : 4-time play 3h : endless play until stop

Stop :
If you want to stop during playing, you can stop play by setting this register high. It is not necessary to reset because it is internally cleared oneself.

- Control1 Register (D-Amp Control Register)

EnDth :
It will use a dither function for sound quality improvement.
0: Disable, 1: Enable

SynDth :
Select dither function mode.
0: Asymmetrical, 1: Symmetrical

AmtDth :
Set the amount of dither.
0h: 18-bit position, 1h: 17-bit position, 2h: 16-bit position, 3h 15-bit position.

EnFlt :
Set the activation of fault protection function in the Speaker Block.
0: Enable, 1: Disable

- Direct Access to Internal Flash ($E4h[7])
EnPgm($E4h[7]) is set, CSB, CLK, SDI & BUSY pin are connected directly to internal Flash memory.

NXD1004A	Internal Flash
CSB(P2)	CS#
CLK(P3)	CLK
SDI(P4)	DI
BUSY(P5)	DO

Stand Alone Operation

Without the microprocessor, NXD1004A can operate as “Stand Alone Operation” with key pad. Stand Alone Operation mode is judged internally without pin configuration.

- Designation of the Phrase for Decoding

It is possible to designate the phrase and sentence by using key0 ~ key11 directly. These keys must be set with Matrix structure to designate 36 phrase or sentence. Also it can select phrase mode or sentence mode by setting SELST pin. (0: Phrase mode, 1: Sentence mode)

When using the key switch, there is an electric and mechanical noise of the switch and this noise induce the malfunction. To prevent this, the key inputs are not accepted during 50ms after previous key inputs. Therefore the recommendation is to press the key over 200ms.

- Volume Control

In Stand Alone Operation, the initial volume level is controlled by the INIT0, INIT1 pin at power on time. The volume level can be changed by selecting the level of the VUP and VDN during the power on. When once pressing the VUP button, the 1dB level of volume will increase. When once pressing the VDN button, the 1dB level will decrease. (Please refer to the volume chart)

INIT1	INIT0	Volume(dB)
0	0	0
0	1	-6
1	0	-12
1	1	-18

- Repetition Play the Phrase

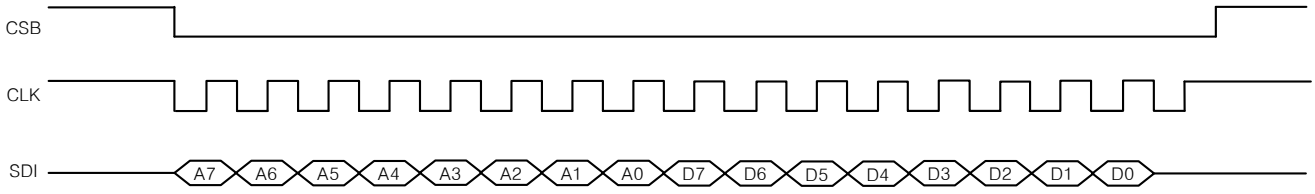
By pushing the RPT pin`s switch, repetition play function is activated. Whenever this pin`s switch is pushed, repetition number is change.(If this switch is pushed 4 times, repetition number is returned 1 time.)

Push Number	Repetition Number
0	1
1	2
2	4
3	Infinity

- Power Save Mode

If there is no play back during over 1second in Stand Alone Operation, the operation will be changed to the Power Save Mode automatically. To play phrase or sentence from power save mode, press any key (key0 ~ key11). In Power Save Mode, the internal clock is stopped and also PWM outputs are off.

MCU Operation by SPI I/F



MCU I/F Timing Chart

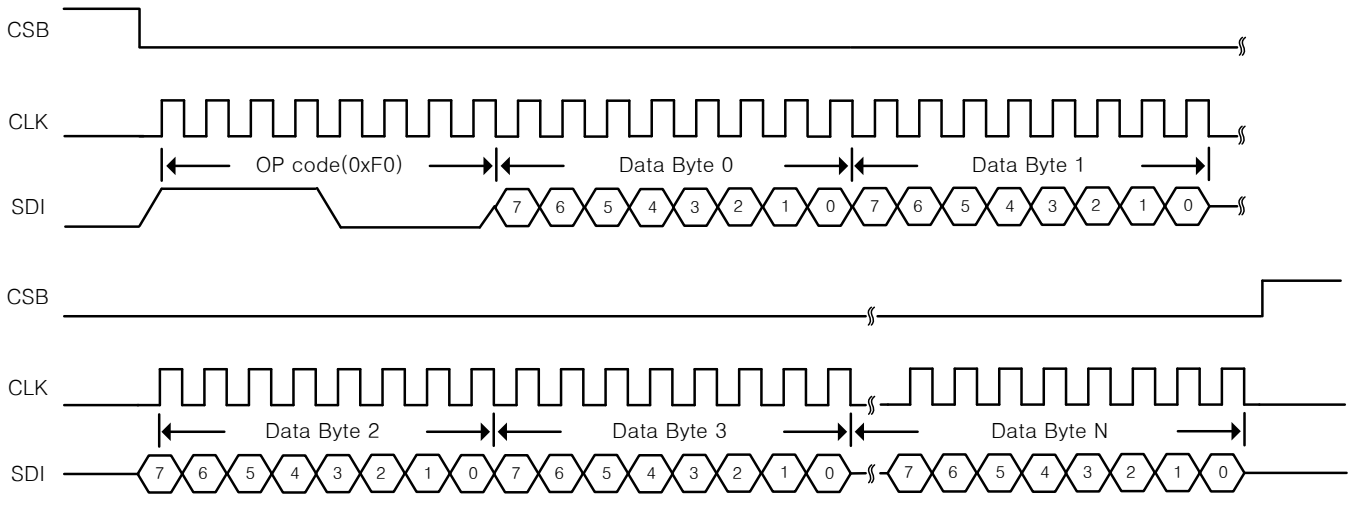
The above is the timing diagram of SPI interface. The structure is composed with the 8 bits address and the 8 bits data. With this SPI interface, MCU controls all the operations. The register control by using the MCU I/F is referenced the Register Map. MCU interface protocol is automatically detected without any pin configurations. CSB goes to High level status for next command. And this CSB signal must be High status during minimum 3us for the stable operation of NXD1004A. For the decoding operation, MCU must observe the BUSY signal of NXD1004A. When the BUSY is High, it means the internal FIFO buffer is full. If the BUSY pin is High-level, this means that there is no space in internal FIFO buffer, therefore can not access the data. Otherwise MCU stops the data writing for a while. If the BUSY is Low-level, MCU can write the data to the NXD1004A for decoding.

- Power Save Mode

If there is no communication with MCU over 1second in MCU Operation, the operation will be changed to the Power Save Mode automatically. To play phrase or sentence from Power Save Mode, please restart to communicate with MCU. In Power Save Mode, the internal clock is stopped and also PWM outputs are Off.

- Direct Play Mode

NXD1003A/1004A is capable to play directly data(Voice and music)that inputted from MCU through SPI interface(CSB, CLK, SDI, BUSY) Data format is such as below diagram.



Data Byte 0 Format

bit	[7:3]	[2]	[1:0]
name	Reserved	encode	Fs[1:0]

1) Fs[1:0] : sampling frequency. 2'b00:4khz, 2'b01:8khz, 2'b10:16khz
2) Encode : encoding of ADPCM. 1'b0:ADPCM, 1'b1:Not encoded
3) Data1 ~ Data N : Real Audio & Voice Data

Internal / External Memory Mode

- Internal Memory Mode

For the decoding the saved ADPCM data within the internal memory, Must come to be converted in proper format with Sampling Frequency 4/8/16KHz(8/16/32KHz). Also non-encoded data can be saved in the internal memory, but playing time is shorter than ADPCM data. After the setting other registers according to the necessity, the decode action will be processed with the selection of the designated phrase. By writing the designation number to Phrase Number Register, the decoding is started.

1) When user set the "0" to the Phrase Number Register, the first phrase is selected.
2) If the designated number is greater than the maximum number of recorded, the phrase that recorded last will be selected.

- External Memory Mode

The user can play the ADPCM or non-encoded data saved in the External Memory. It is available with controlling the register in NXD1004A by MCU. The format of ADPCM files which are stored in the external flash memory is compressed at 4 bit and sampling frequency 4/8/16kHz(8/16/32KHz) are possible. File conversion is a possibility of doing with NXD1003A/NXD1004A PC program. The overall sequence is same as Play ADPCM Data. Also 16 bit PCM data must come to be converted with sameness rightly in NXD1003A/NXD1004A formats. We recommend you use non-encoded data in direct play for a quality.

Data Access to Internal Flash Memory

- Data download sequence

- Internal/external flash program mode setting(address E2h, data 01h)
- Flash Write protection clear operation(address 01h, data 00h)
- Flash chip erase operation(data C7h)
- Flash page program operation(Refer to figure3 on 12page.)
- Flash Write protection setting(address 01h, data 9Ch)
- Internal/external flash memory play mode setting(address E2h, data 00h)

- Write Enable(06h)

The Write Enable instruction (Figure 1) set the Write Enable Latch bit. The Write Enable Latch bit must be set prior to every Page Program(PP), Sector Erase(SE), Block Erase(BE, Chip Erase(CE), and Write Status Register instruction.

The Write Enable instruction is entered by driving Chip Select(CSB) low, sending the instruction code, and then driving Chip Select(CSB) high.

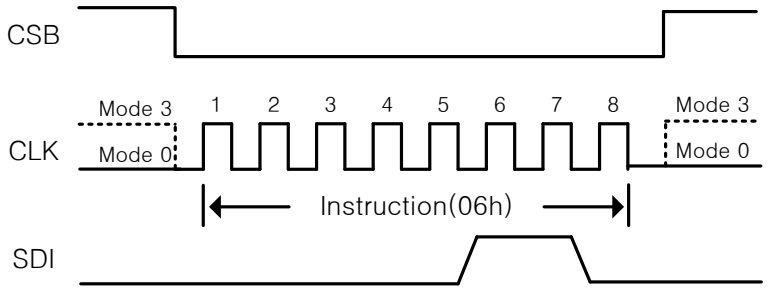


Figure 1. Write Enable instruction Sequence Diagram

- Write Status Register(01h)

The Write Status Register instruction allows new value to be written to the Status Register. Before it can be accepted, a Write Enable instruction must previously have been executed. After the Write Enable instruction has been decoded and executed, the device sets the Write Enable Latch.

The Write Status Register instruction is entered by driving Chip Select (CSB) low, followed by the instruction code and the data byte on Serial Data Input (SDI).

The instruction sequence is shown in Figure 2.

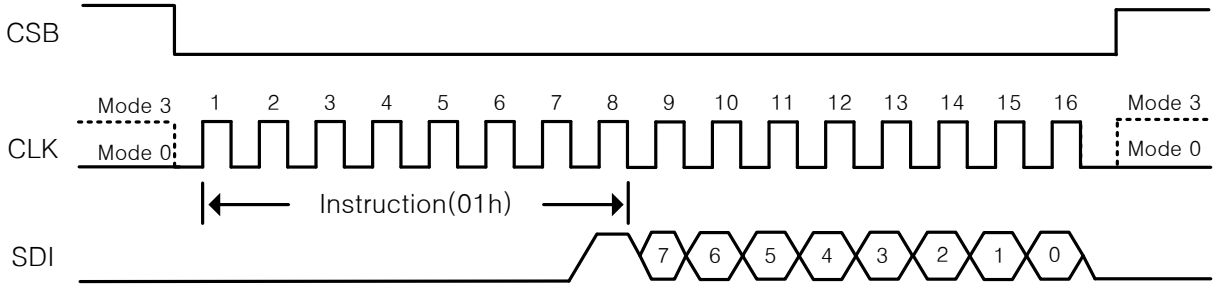


Figure2. Write Status Register Instruction Sequence Diagram

- Page Program(PP) (02h)

The Page Program(PP) instruction allows bytes to be programmed in the memory. Before it can be accepted, a Write Enable instruction must previously have been executed. After the Write Enable instruction has been decoded, the device sets the Write Enable Latch.

The Page Program(PP) instruction is entered by driving Chip Select(CSB) low, followed by the instruction code, three address bytes and at least one data byte on Serial Data Input(SDI). If the 8 least significant address bits (A7 – A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page(from the address whose 8 least significant bits (A7 –A0) are all zero). Chip Select(CSB) must be driven low for the entire duration of the sequence.

The instruction sequence is shown in Figure 3. If more than 256bytes are sent to the device, previously latched data are discarded and the last 256 data bytes guaranteed to be programmed correctly within the same page. If less than 256 Data byte are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

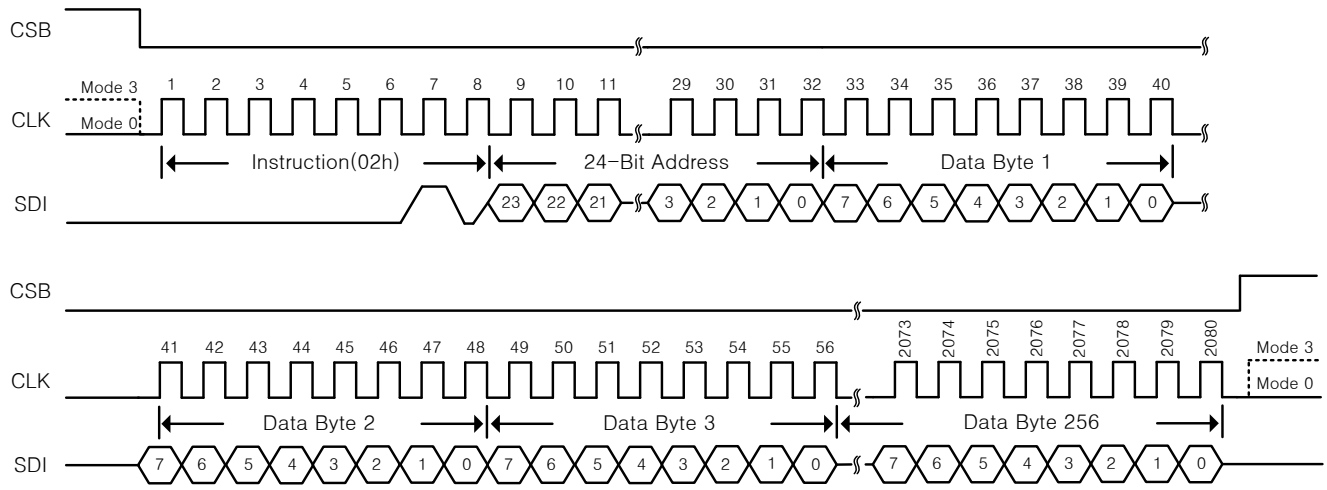


Figure 3. Page Program Instruction Sequence Diagram

- Sector Erase(SE) (20h)

The Sector Erase(SE) instruction sets to 1(FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable instruction must previously have been executed. After the Write Enable instruction has been decoded, the device sets the Write Enable latch.

The Sector Erase(SE) instruction is entered by driving Chip Selcet(CSB) low, followed by the instruction code, and three address bytes on Serial Data Input(SDI). The instruction sequence is shown in Figure 4.

Chip Select(CSB) must be driven high after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase(SE) is not executed.

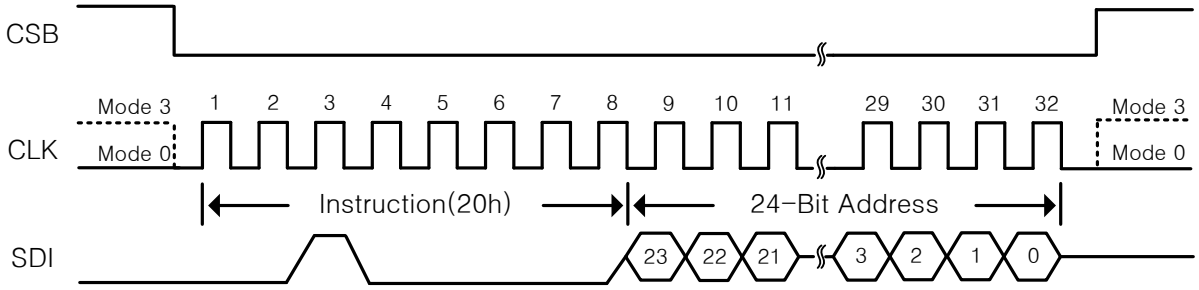


Figure 4. Sector Erase Instruction Sequence Diagram

- Block Erase(BE) (D8h)

The Block Erase(BE) instruction sets to 1 (FFh) all bits inside the chosen block. Before it can be accepted, a Write Enable instruction must previously have been executed. After the Write Enable instruction has been decoded, the device sets the Write Enable latch.

The Block Erase(BE) instruction is entered by driving Chip Select(CSB) low, followed by the instruction code, and three address bytes on Serial Data Input(SDI).

The instruction sequence is shown in Figure 5. Chip Select(CSB) must be driven high after the eighth bit of the last address byte has been latched in, otherwise the Block Erase(BE) is not executed.

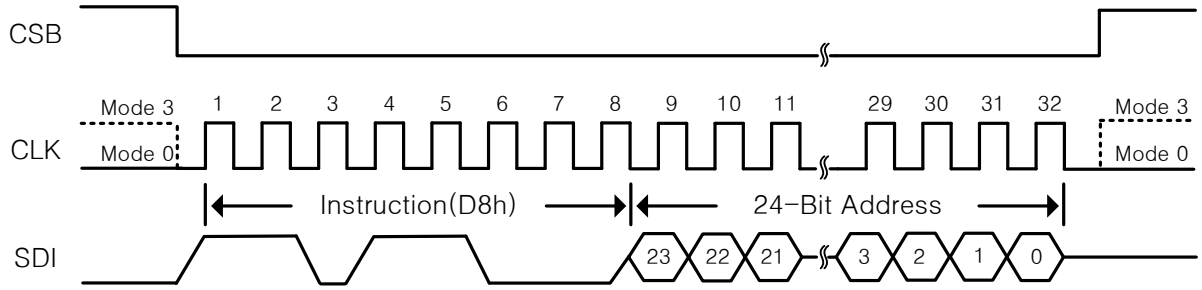


Figure 5. Block Erase Instruction Sequence Diagram

- Chip Erase(CE) (C7h)

The Chip Erase(CE) instruction sets all bits to 1(FFh). Before it can be accepted, a Write Enable instruction must previously have been executed. After the Write Enable instruction has been decoded, the device sets the Write Enable latch.

The Chip Erase(CE) instruction is entered by driving Chip Select(CSB) low, followed by the instruction code on Serial Data Input(SDI). Chip Select(CSB) must be driven low for the entire duration of the sequence.

The instruction sequence is shown Figure 6. Chip Select(CSB) must be driven high after the eighth bit of the instruction code has been latched in, otherwise the Chip Erase instruction is not executed.

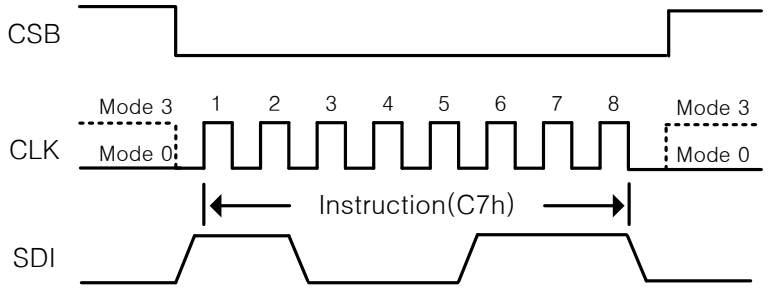


Figure 6. Chip Erase Instruction Sequence Diagram

Flash Memory Map

- Phrase Table (Address 0x000000 ~0x0017FF)

The Phrase Table is Pointer map concerning phrase audio data.
Phrase number is totally 255 from 0 to 254 and phrase number 255 is not available.
Phrase group number is totally 8 of 255 phrases
One Phrase is consist of 3 bytes (High byte, Middle byte, Low byte)
Phrase Table 0(Phrase group 1) is shown in Figure 1.

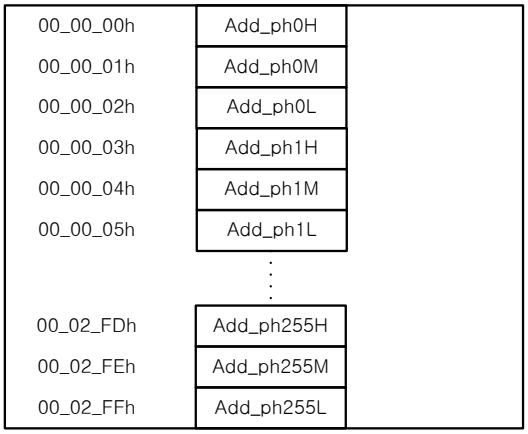


Figure 1. Phrase Table Diagram

- Sentence Table (Address 0x001800 ~0x0057FF)

The Sentence Table is capable to use maximum 8 phrase. If sentence use less than 8 phrases, you should program 0xFF behind the last phrase. You can use totally 2048 sentence number.
Sentence Table is shown in Figure 2.

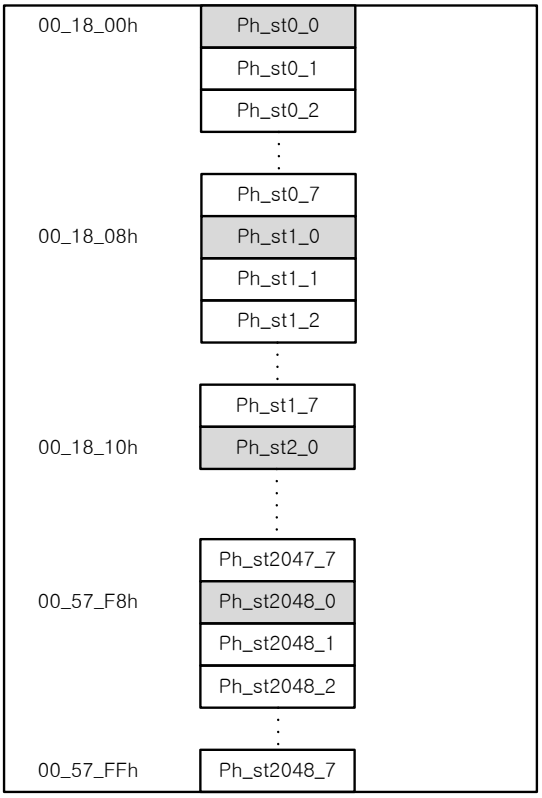
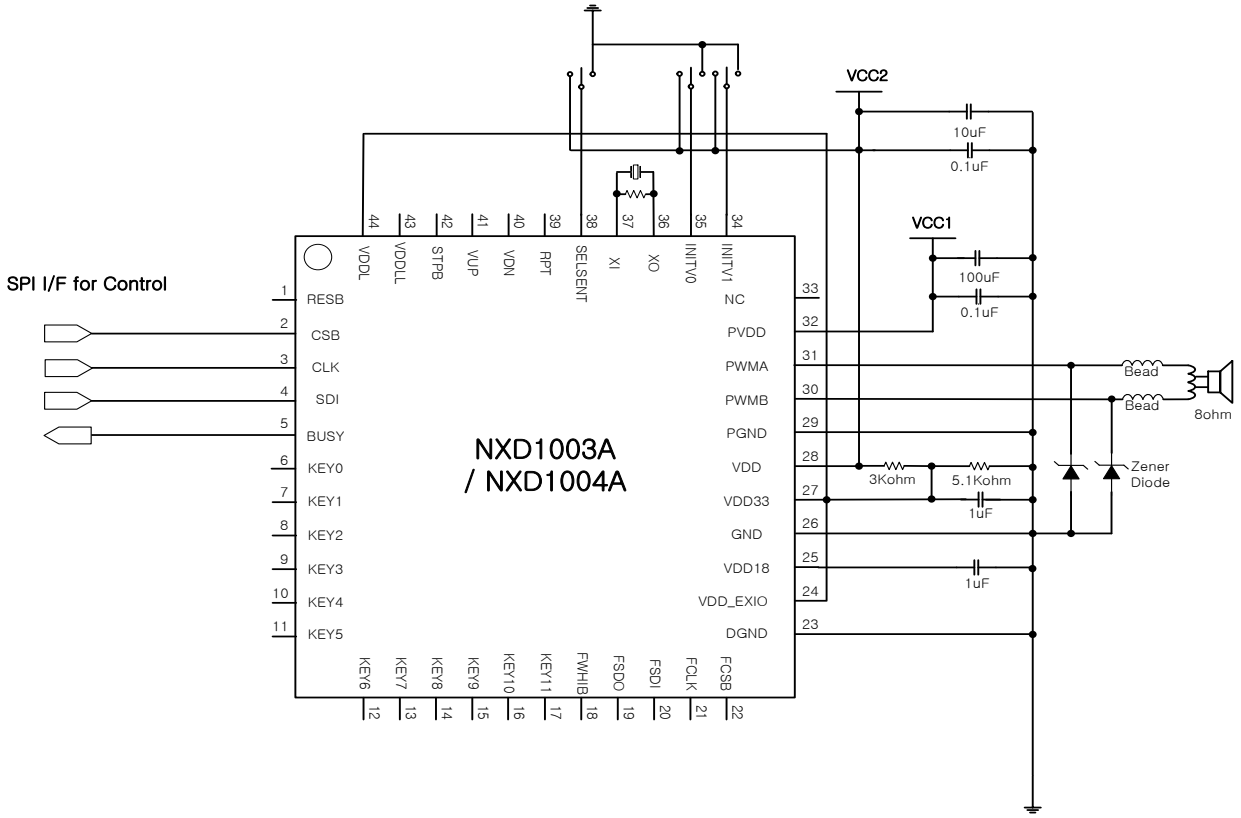


Figure 2. Sentence Table Diagram

Application

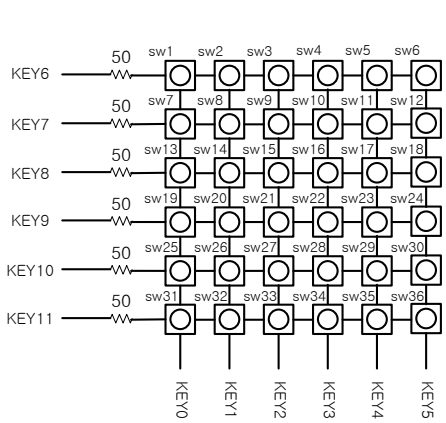
- Test circuit

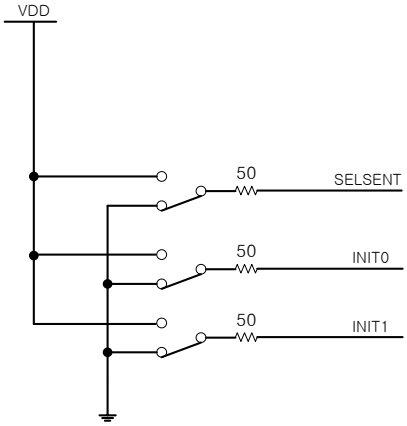


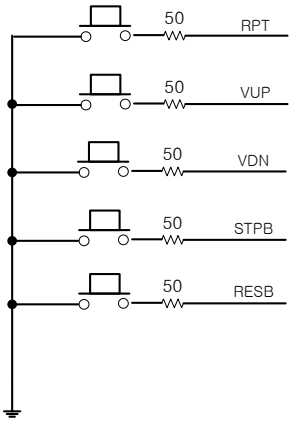
※ Power capacitor(Capacitor fo PVDD, VDD, VDD33 & VDD18) should be affixed as close as possible in the IC.

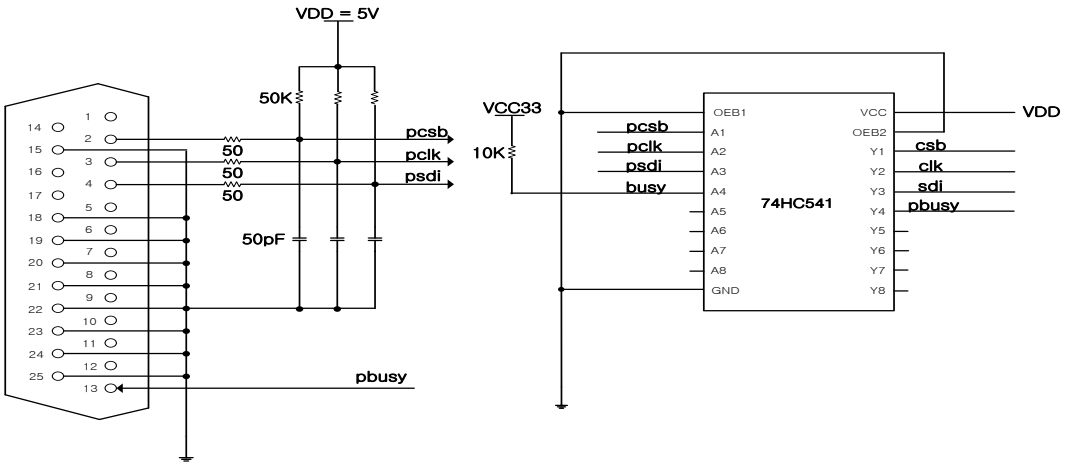
※ Zener Diode and Bead are optional parts for Field Reliability Test (EDS Test).

※ Recommendation : Zener Diode -1N5231B, Bead - EBMS201209B202









※ In case that, Internal Flash Memory should be supplied with 1.8V power in further application, VDD18 pin must be connected to VDDLL.

With connecting VDD_EXIO and VDD(External Flash Memory`s Power), It can support the compatibility against Memory`s power usage.

VCC1 and VCC2 are same voltage but It should be separated to avoid resetting IC.
If it is connected directly between VDD(#28) and PVDD(#32), there is a possibility to be reset because of current consumption of PVDD(#32). So we recommend that Power line is separated in drawing PCB.

- Play Monitor Option

It is available to check playing status with Play Monitor Option.

Address E3h, data 05h : Play Monitor Enable, data 00h : Play Monitor Disable.

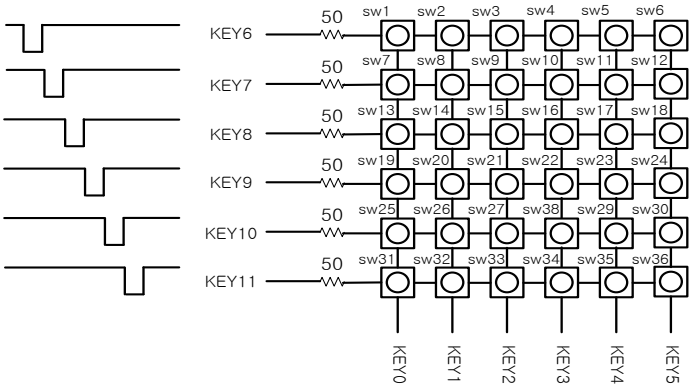
Address E2h, data 60h : Play Signal Monitor Pin Mapping.

It can check playing status through Pin KEY11 (#17).

KEY11 is “High” while playing and KEY11 is “Low” when stop playing.

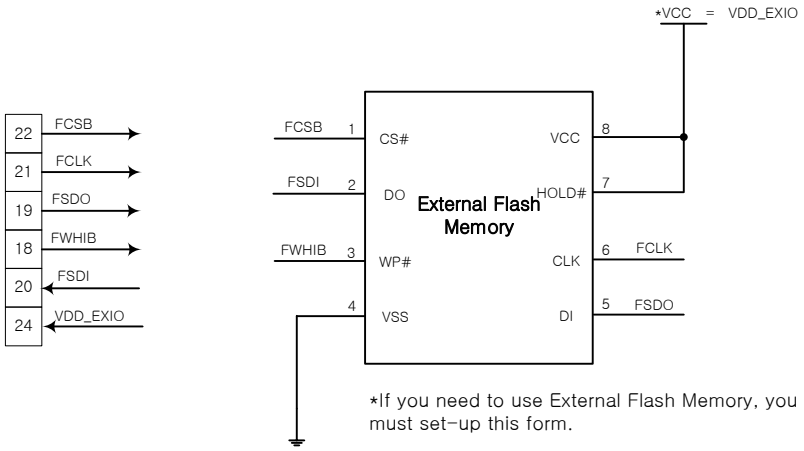
In Play Monitor Option, Pin INITV0(#35) and INITV1(#34) are Output pins. In the case that these pins are connected to VCC, GND or u-com output, insert the 5K resistors to input stage of these pins for prevention the unwanted current.

- Matrix Method Diagram



In operation mode, Output keys(key6 ~ key11) outputs signals such an above diagram. Namely when output key`s status is low level, NXD1004A can detect the status of input keys(key0 ~key5).

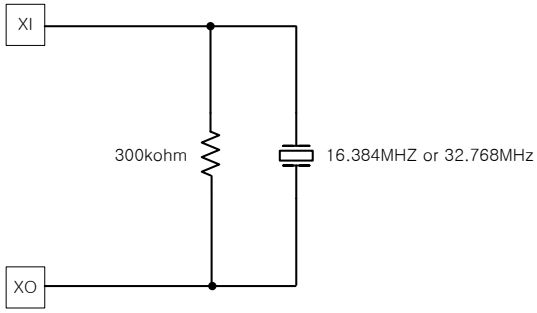
- External Flash Memory SPI I/F Diagram



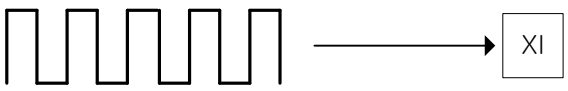
※ VDD pin(External Flash Memory Power) must be connected with VDD_EXIO pin to avoid problem about the confusion between internal VDD and external VDD.

- X-tal usage recommendation

In case of using X-tal (We recommend that you should use this method as possible.)
We recommend that you should use below X-tal.
(Company:SUNNY, Frequnecy:16.0MHz, Frequency Tolerance:±50ppm, C_L(Load Capacitance):18pF)



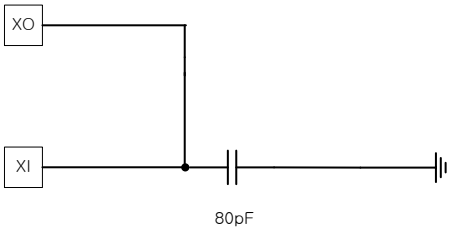
In case of using system clock (Recommended Frequency Fr = 16.384MHz or 32.768MHz)



System clock(16.384MHZ or 32.768MHz)

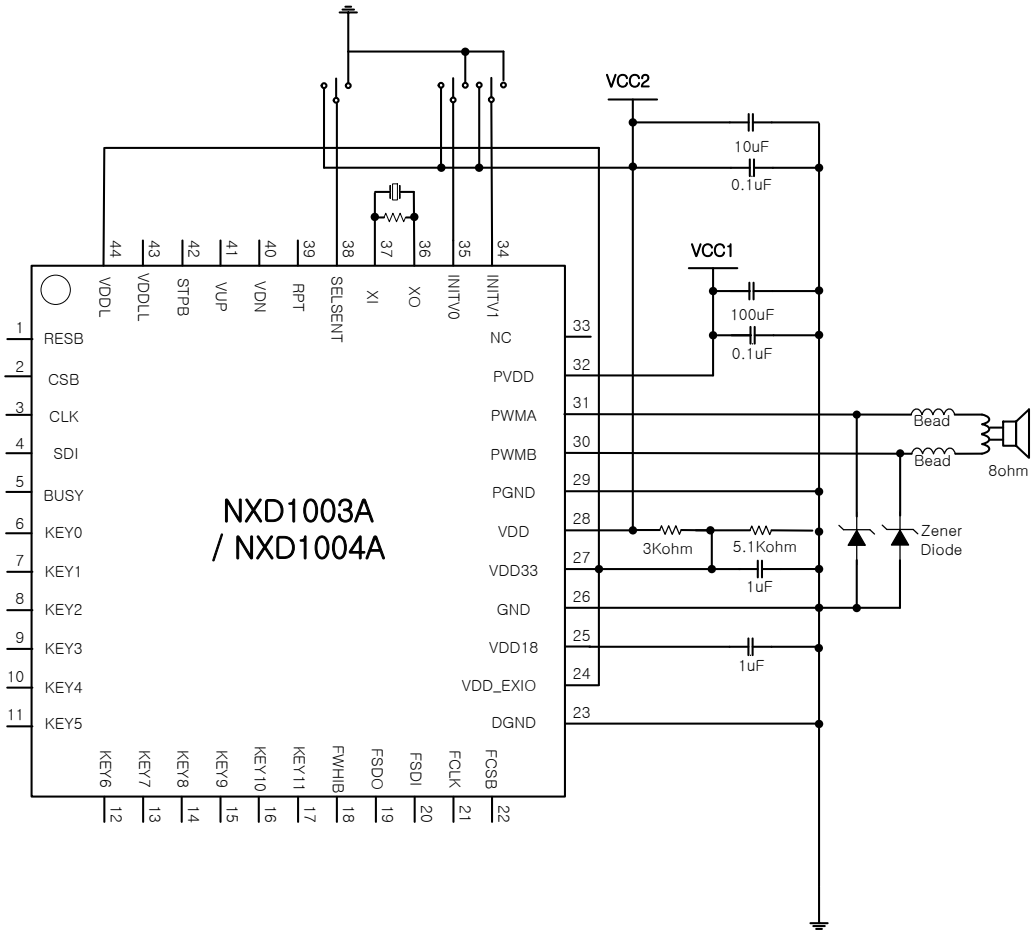
* If clock is being used in the system, NXD1003/1004 can use this clock source directly with connecting to XI pin.

In case of using resistor and capacitor



There is possibility to be changed of capacitor value depending PCB pattern.

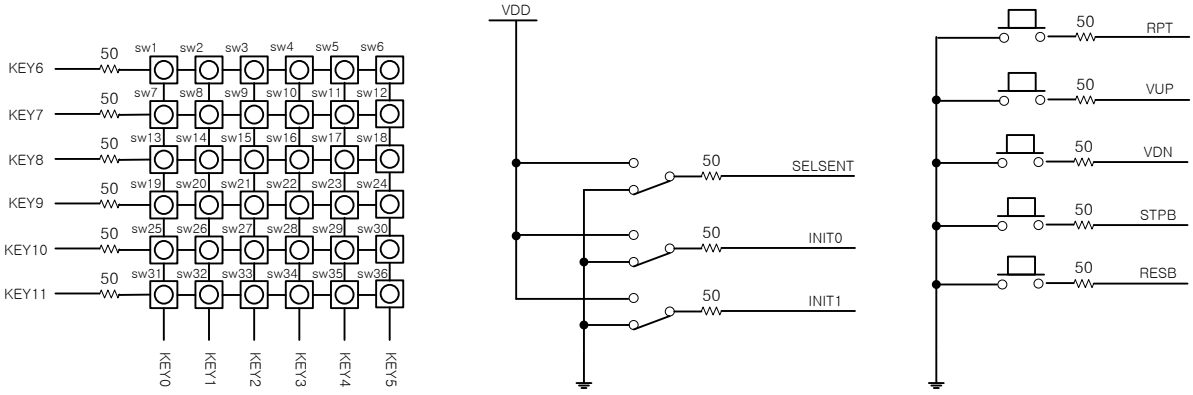
- Stand alone application

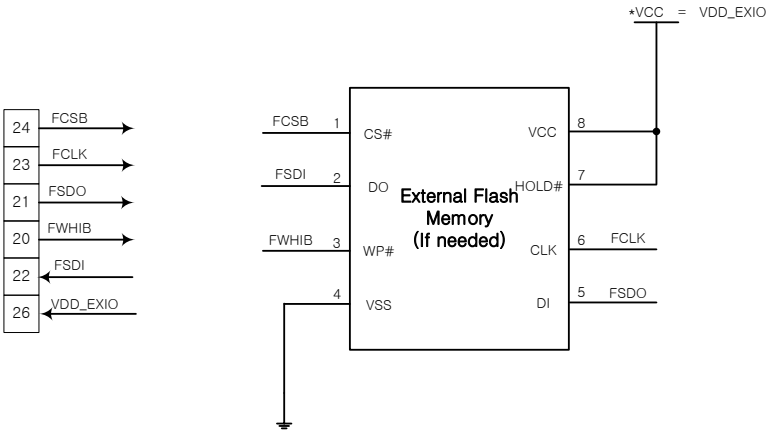


※ Power capacitor(Capacitor fo PVDD, VDD, VDD33 & VDD18) should be affixed as close as possible in the IC.

※ Zener Diode and Bead are optional parts for Field Reliability Test (EDS Test).

※ Recommendation : Zener Diode -1N5231B, Bead - EBMS201209B202





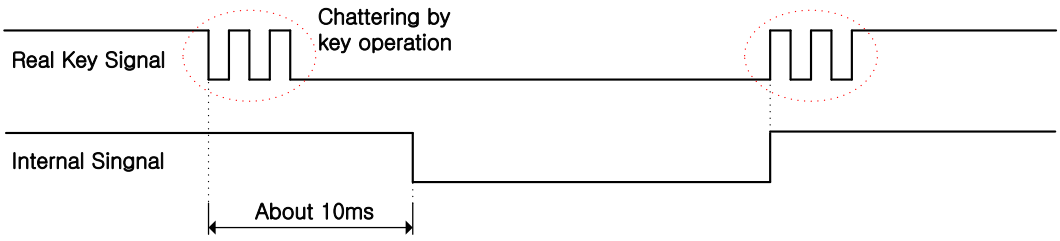
From Stand Alone Operation, the decoding is accomplished key switch. NXD1003A/1004A is equipped with 6 input key (key0 ~ key5) and 6 output key6 (key6 ~ key11). It can designate 36 phrase with time sharing by output keys. Also it is equipped with volume control pin(VDN and VUP). When VDN key is pressed one time, the volume decreases 1dB. And when VUP key is pressed one time, the volume increases 1dB. Initial Volume is enable to be set with INIT0 and INIT1 pin at the power-on time. After power-on, these pin`s status does not affect to the volume level.

It is enable to operate play for repetition by setting RPT pin`s switch. Whenever this pin`s switch is pushed, repetition number is change.(If this switch is pushed 4 times, repetition number is returned 1 time.)

STPB controls stop function during the playing phrase. This action is operated with setting one`s status “Low”.

From Stand Alone Operation, when the decoding action for the selected file is completed, NXD1004A goes to the clock stop mode. If the one of key(key0 ~ key11) is pressed, the internal clock wake and then operate.

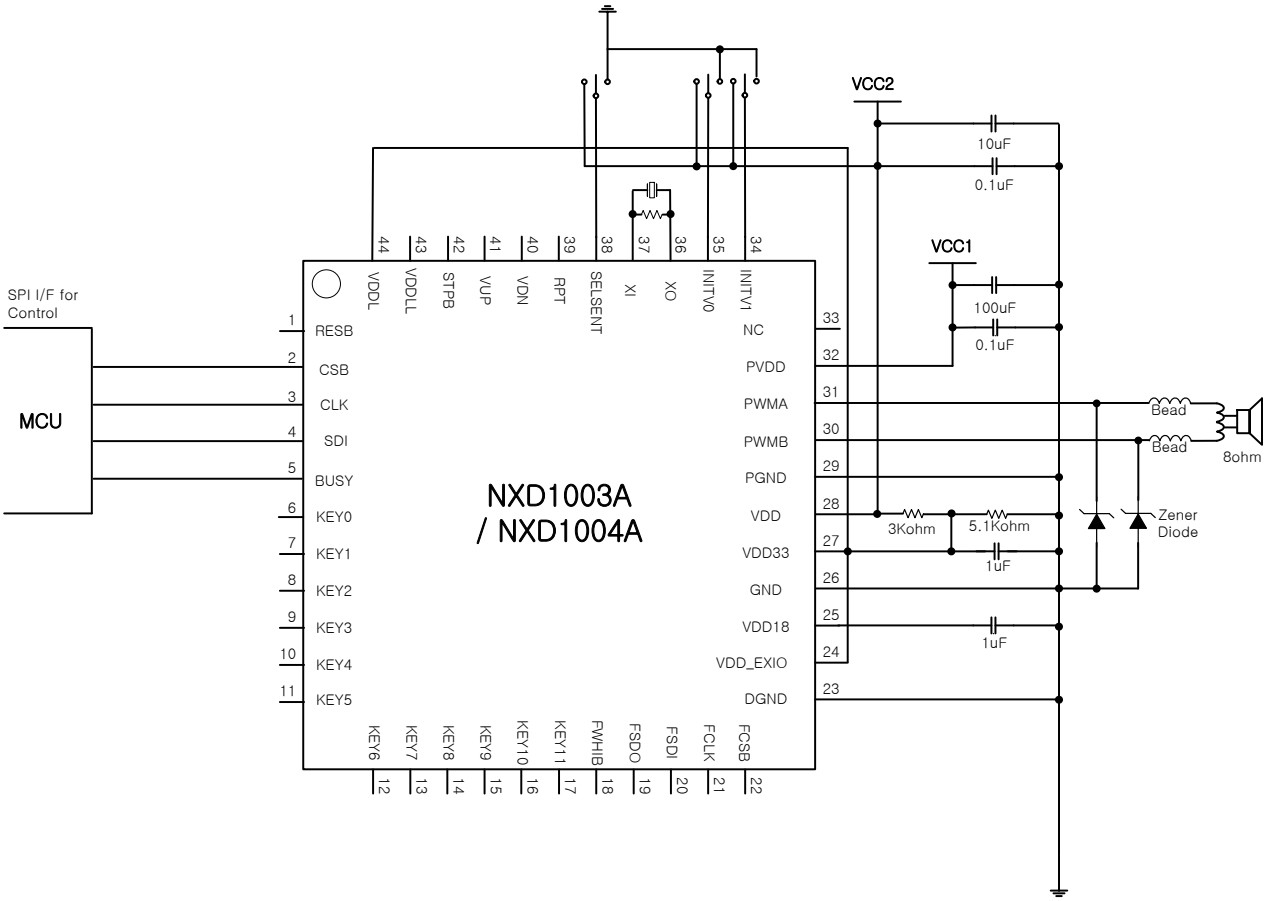
Key Operation in Standalone Mode



When using the key switch, there is an electric and mechanical noise of the switch such an above diagram and this noise induces the malfunction.

To prevent this malfunction, NXD1003A/1004A outputs Internal Signal delayed 10ms from key operation. When key operation is ended, Internal Signal is change to “High” right.

- MCU application



※ Power capacitor(Capacitor for PVDD, VDD, VDD33 & VDD18) should be affixed as close as possible in the IC

※ Zener Diode and Bead are optional parts for Field Reliability Test (EDS Test).

※ Recommendation : Zener Diode -1N5231B, Bead - EBMS201209B202

※Caution

There is no need the pull-up resistor for KEY0~KEY5 pin.

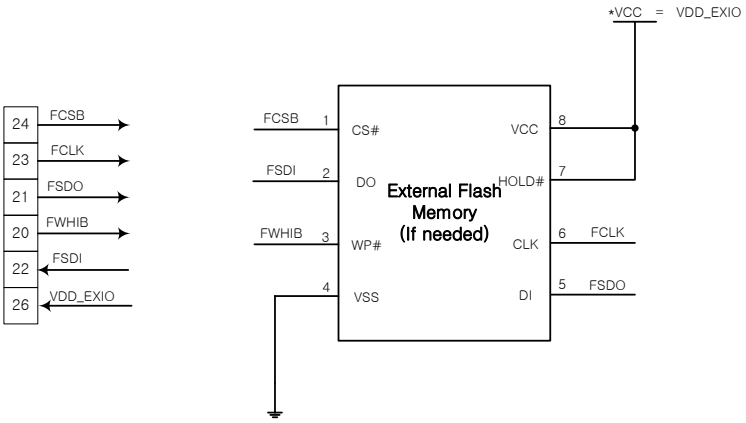
Because NXD1003A/1004A has internally pull-up for these, therefore if you connect to ground(GND), the unwanted current flows and increases the power consumption.

If you want to play phrase and sentence by turns, MCU should control SELSENT(41). If the status of SELSENT is changed, it is applied from next turn.

You Should monitor VDD33(#27) to confirm playing status.

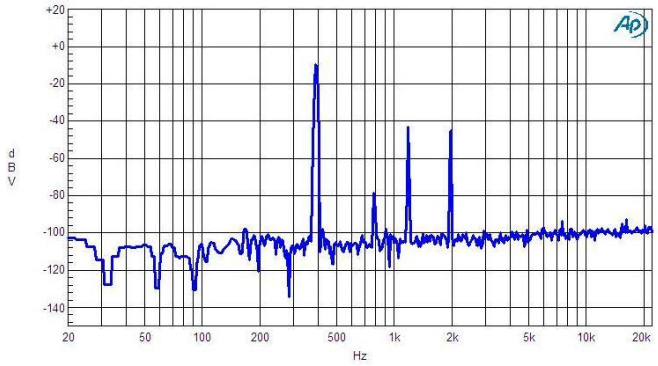
In case of External flash application, you should connect flash`s VDD to VDD33(#27)

Internal LDO is enough to drive flash memory, also you should connect VDD_EXIO(#24) to VDD33(#27)

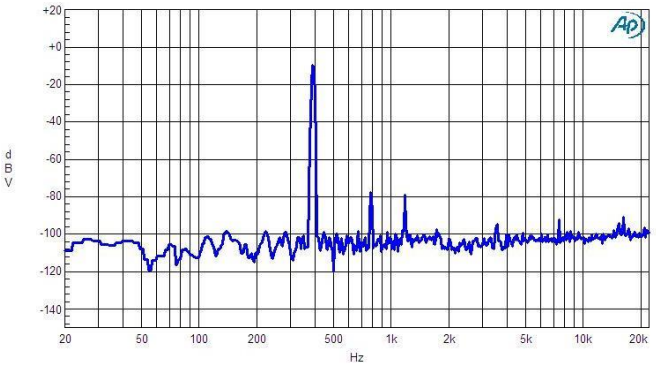

*VCC = VDD_EXIO
24 FCSB
23 FCLK
21 FSDO
20 FWHIB
22 FSDI
26 VDD_EXIO
FCSB 1
CS#
FSDI 2
DO
FWHIB 3
WP#
4
VSS
VCC 8
HOLD# 7
CLK 6 FCLK
DI 5 FSDO
External Flash
Memory
(If needed)

FFT Waveform

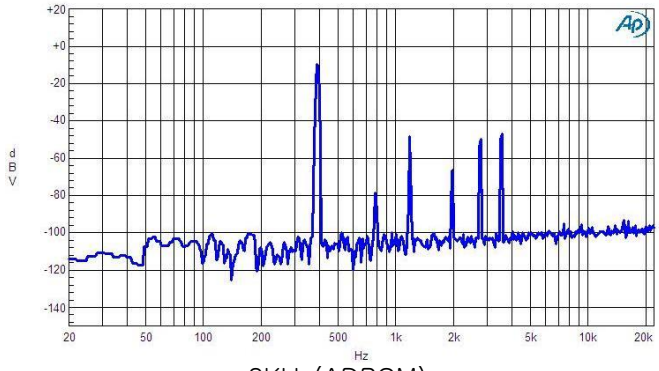
- Gain (-10dB) , Sine Wave(400Hz)



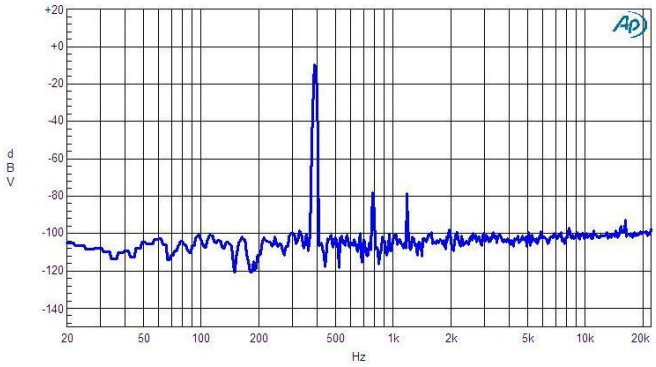
4KHz(ADPCM)



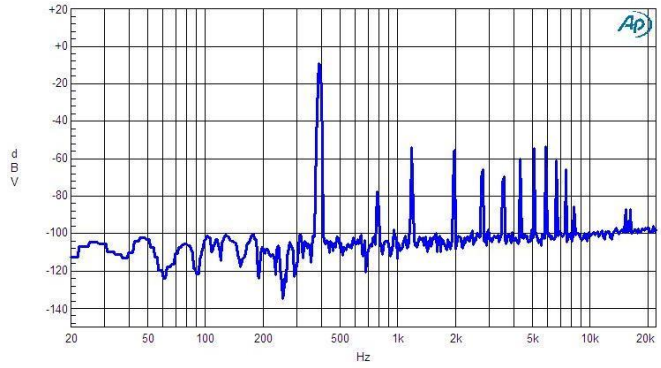
4KHz(Linear)



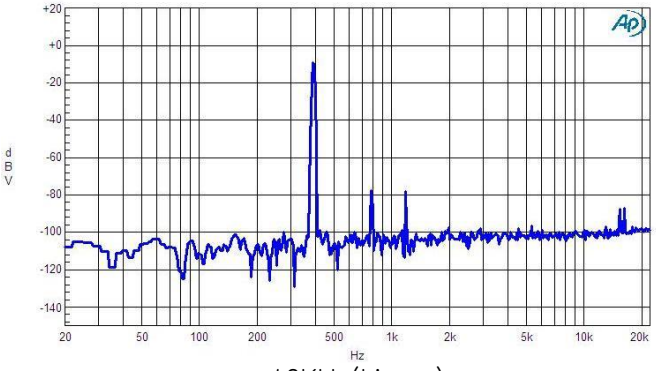
8KHz(ADPCM)



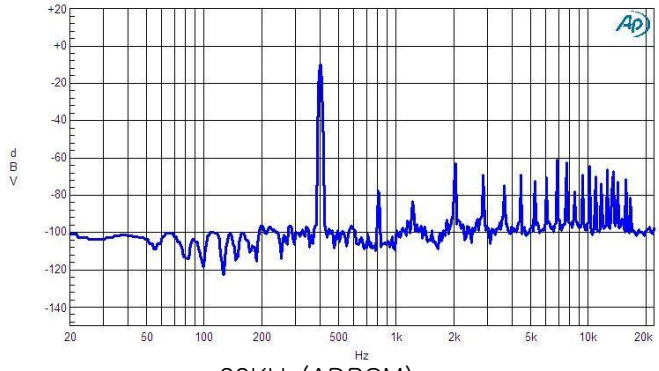
8KHz(Linear)



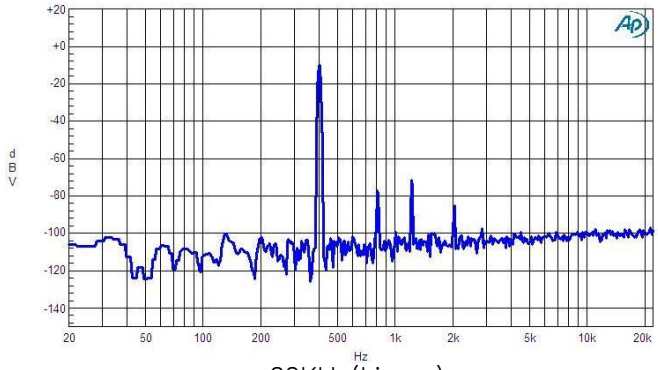
16KHz(ADPCM)



16KHz(Linear)

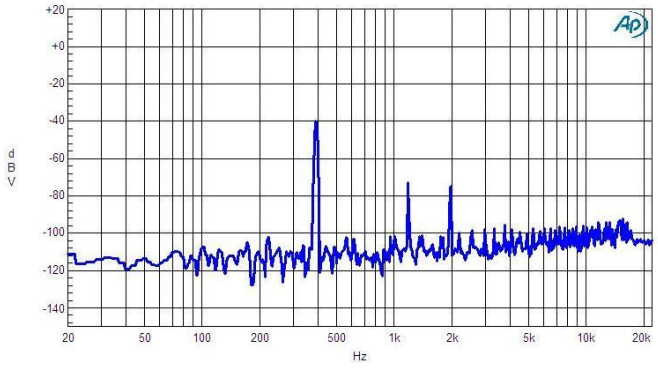


32KHz(ADPCM)

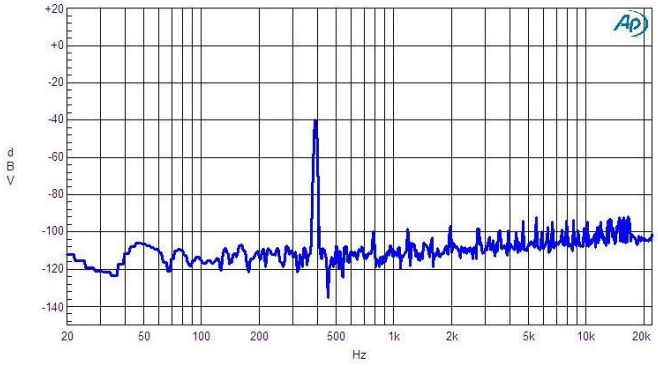


32KHz(Linear)

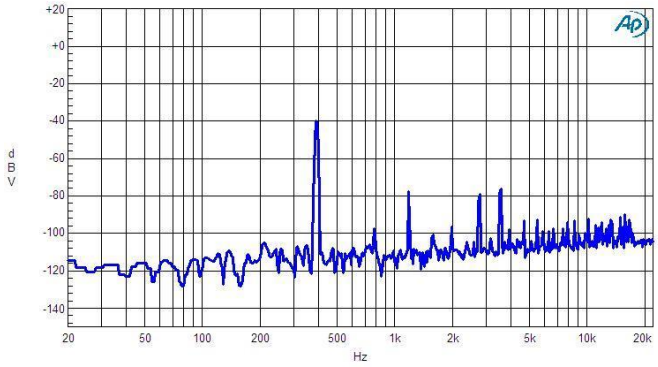
- Gain (-40dB) , Sine Wave(400Hz)



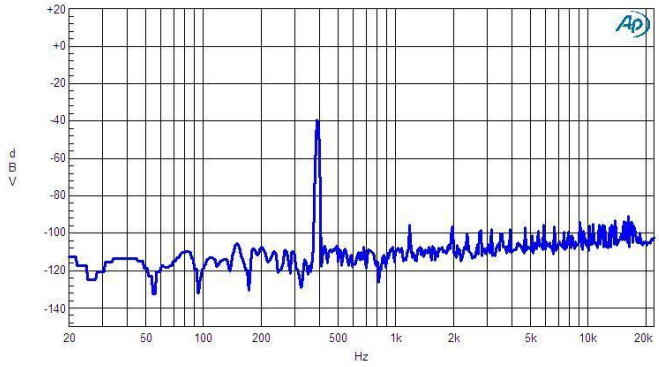
4KHz(ADPCM)



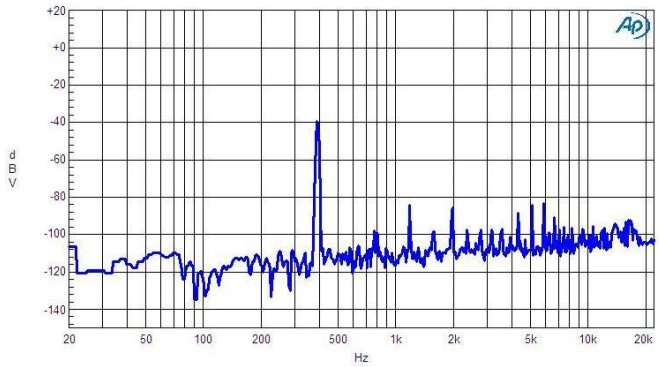
4KHz(Linear)



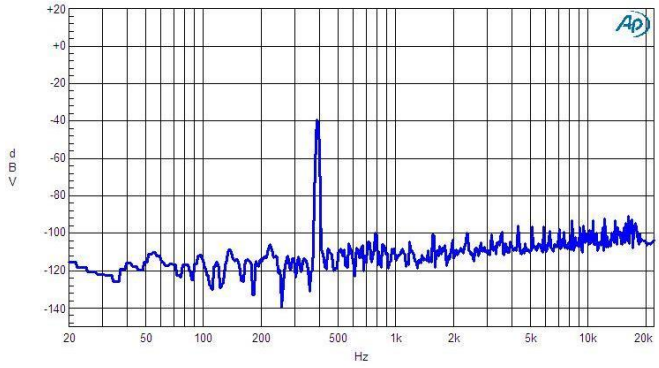
8KHz(ADPCM)



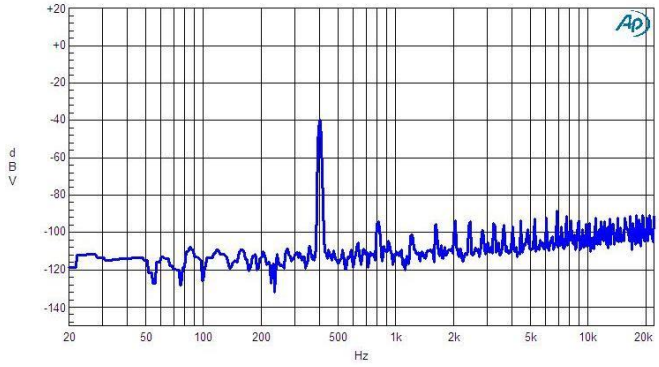
8KHz(Linear)



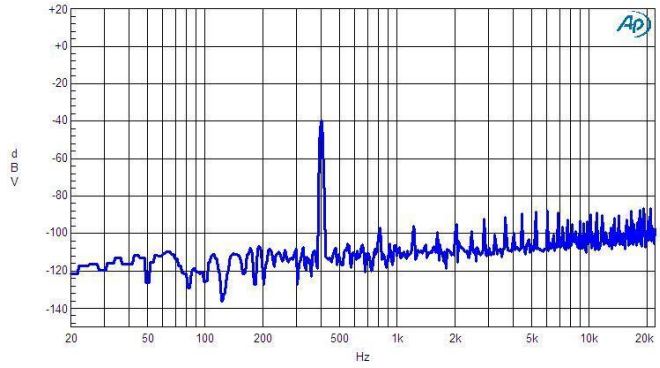
16KHz(ADPCM)



16KHz(Linear)

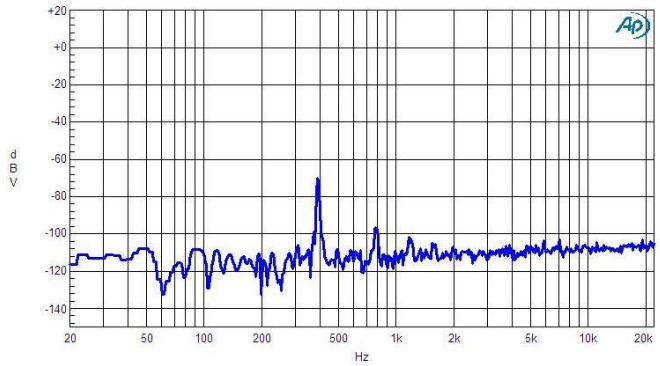


32KHz(ADPCM)

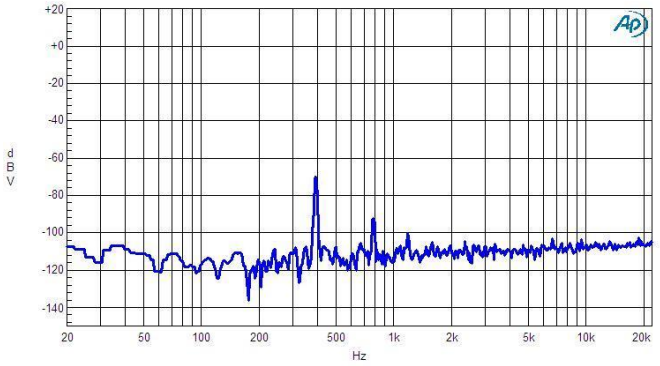


32KHz(Linear)

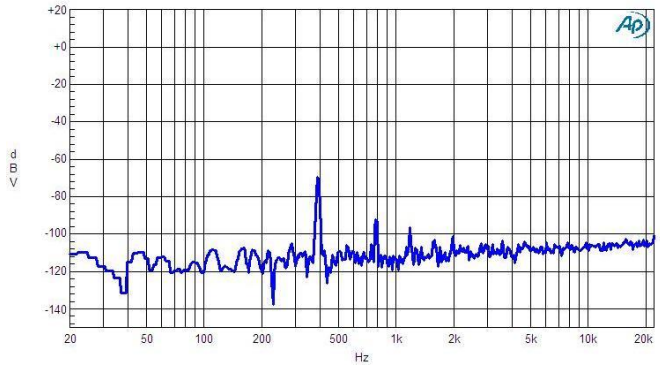
- Gain (-70dB) , Sine Wave(400Hz)



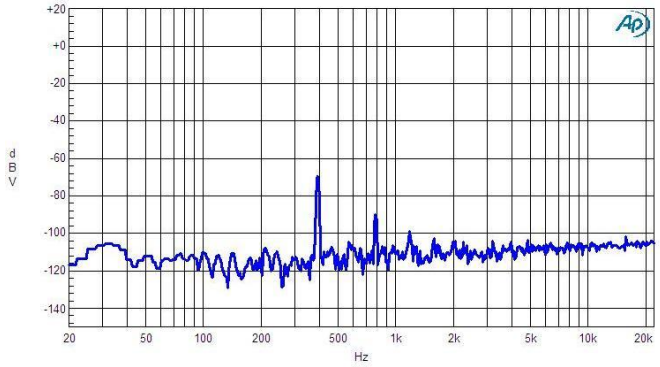
4KHz(ADPCM)



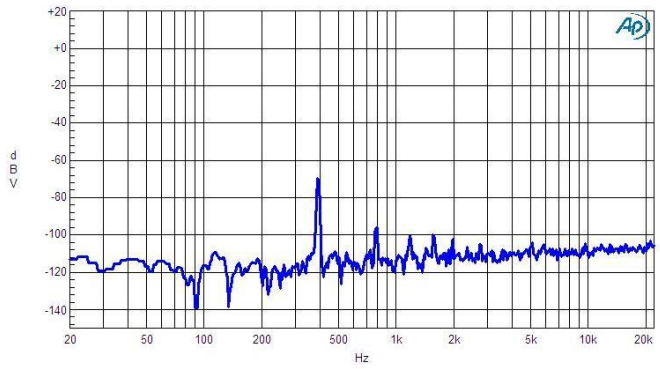
4KHz(Linear)



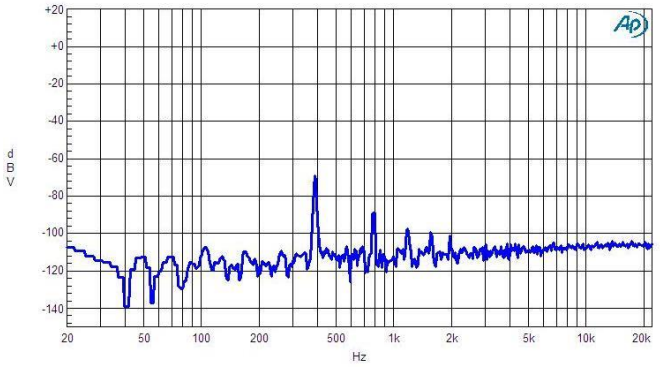
8KHz(ADPCM)



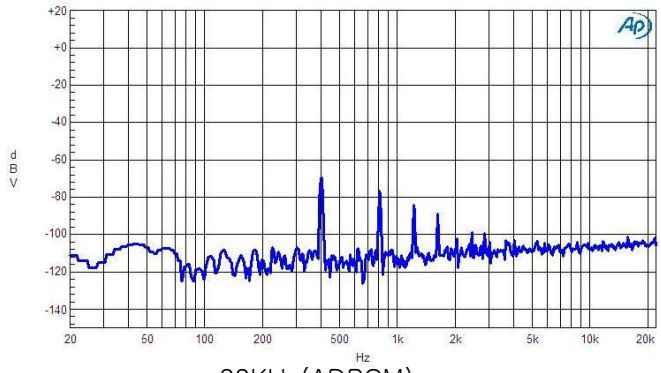
8KHz(Linear)



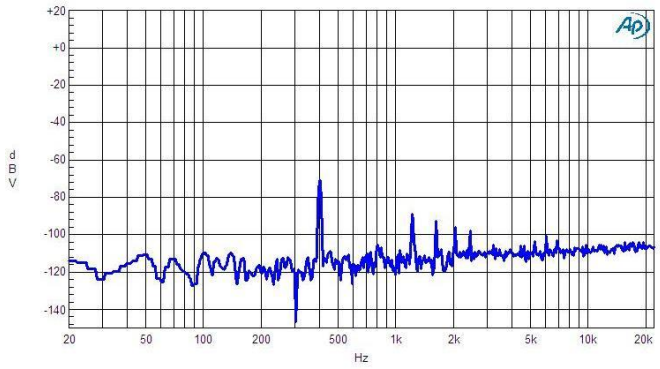
16KHz(ADPCM)



16KHz(Linear)

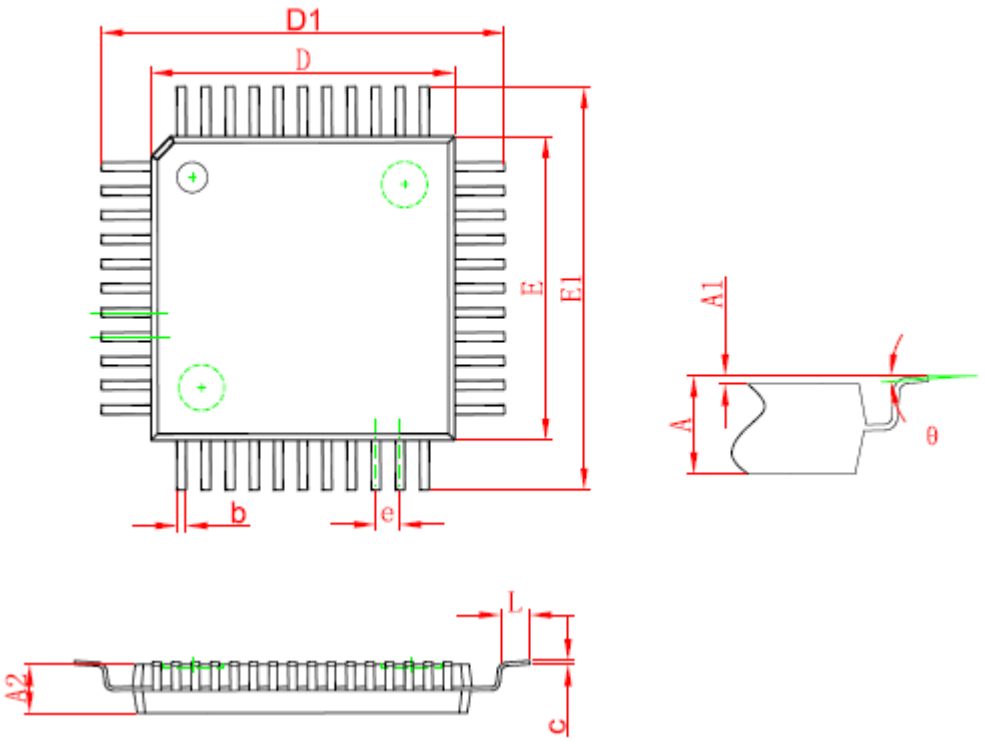


32KHz(ADPCM)



32KHz(Linear)

Package Dimensions <44QFP>



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.600		0.063
A1	0.050	0.150	0.002	0.006
A2	1.350	1.450	0.053	0.057
b	0.280	0.400	0.011	0.016
c	0.100	0.200	0.004	0.008
D	9.900	10.100	0.390	0.398
D1	11.850	12.150	0.467	0.478
E	9.900	10.100	0.390	0.398
E1	11.850	12.150	0.467	0.478
e	0.800 (BSC)		0.031 (BSC)	
L	0.450	0.750	0.018	0.030
θ	0°	7°	0°	7°